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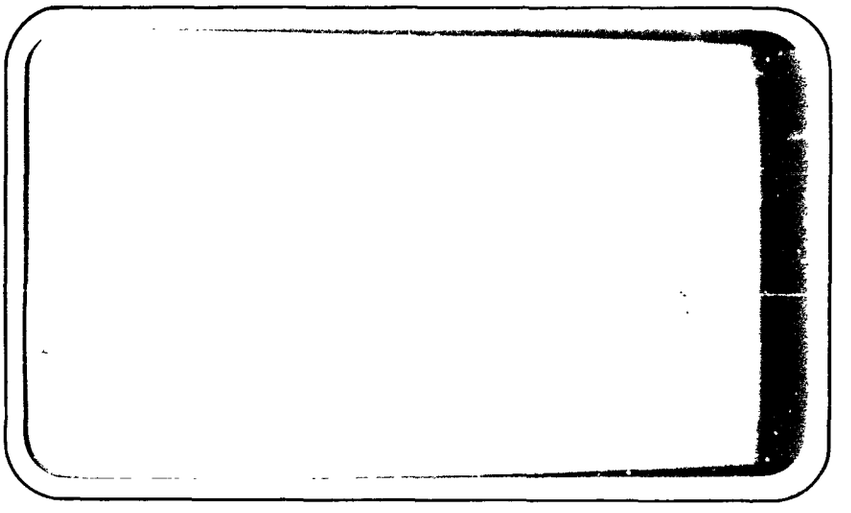

Westinghouse

ELECTRIC CORPORATION

FINAL REPORT
FOR A

Redundant Spacecraft Sequencer Breadboard

For The Period March 30, 1966 to June 30, 1966

NASA Contract NAS 7-100
Task Order RD-30
JPL Subcontract 951345
Westinghouse LAD-38552

Prepared For:

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Summary

This report describes work performed during Phase I and Phase II of JPL subcontract number 951345. This program has included the completion of design detail, the implementation, and the test of a redundant spacecraft sequencer breadboard. The sequencer breadboard is a redundant version of a portion of the Mariner C Spacecraft Sequencer as described previously in the Task II report of JPL subcontract 950777, "Design Study for a Redundant Spacecraft Sequencer."

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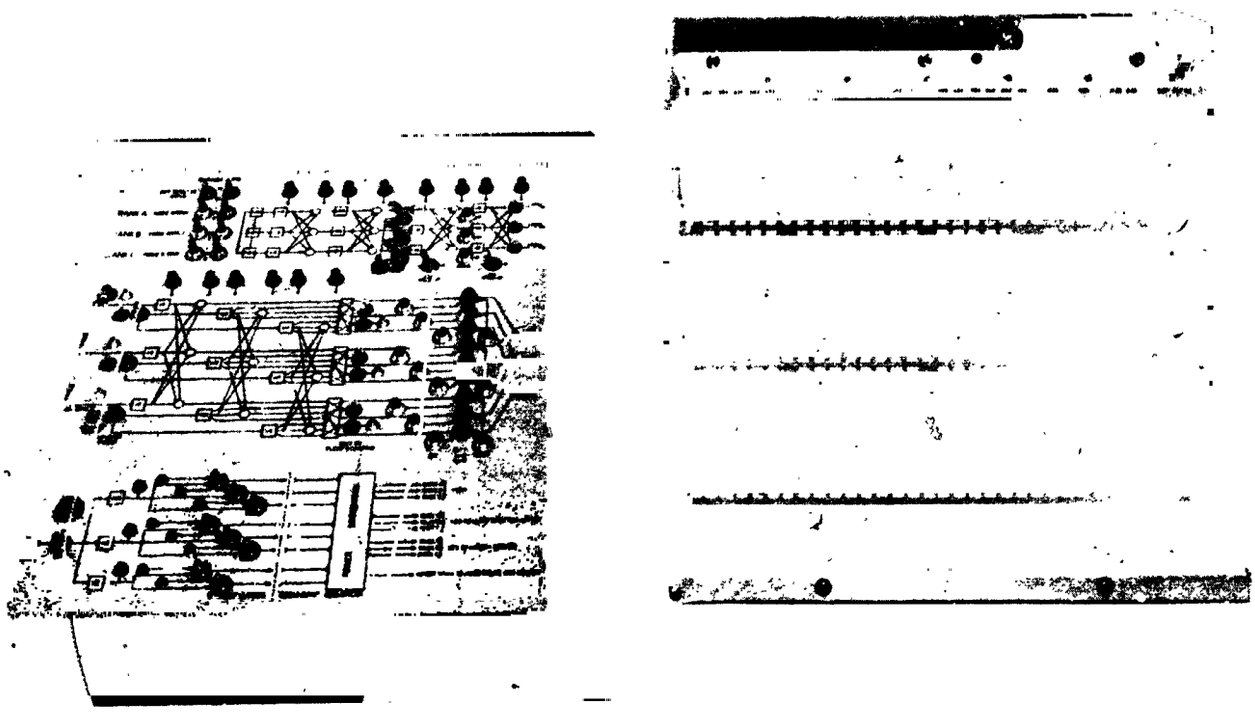

Figure 1-0. Redundant Spacecraft Sequencer Breadboard

1. Introduction

This report is the final report in a two phase program for the fabrication and test of a Redundant Spacecraft Sequencer. This program is a follow-on to a previous design study performed by Westinghouse on JPL subcontract 950777. In the design study, a computer synthesis procedure was used to design a redundant version of the Central Computer and Sequencer of the Mariner C spacecraft. This equipment was to be subject to all of the functional requirements of the non-redundant central computer and sequencer plus the following additional requirements:

1. No single component failure could cause the failure of any critical event output.
2. The equipment was required to be non-volatile so that in the event of a power failure it would not lose significant information and would resume operation in the usual manner when power was restored.

The basic function of the central computer and sequencer is to provide timing signals to other subsystems of the spacecraft. These signals are primarily in the form of relay closures and are used to control the spacecraft midcourse maneuvers, as well as to initiate other events which occur throughout the mission. The study resulted in an equipment design which promised to afford a significant reliability improvement over an equivalent non-redundant equipment. This improvement is achieved with very little weight increase over that required by basic triplication of the non-redundant circuitry. The design makes use of multiple-line logic, with three copies of each logical design and majority voting circuits at selected points to remove the effects of errors.

The breadboard model, developed during the present contract, verifies the sequencer design approach and demonstrates the effectiveness of the redundancy. The breadboard includes the electrical equivalent of a significant portion of the entire redundant sequencer. Low density packaging was used to reduce costs and to permit a comprehensive testing program to be performed. The circuitry is a combination of integrated and discrete component circuits. The first phase of this program involved the finalization of the breadboard design and establishment of an effective test plan. The second phase included the fabrication and testing of the system.

A simplified block diagram of the portion of the central computer and sequencer which has been implemented is shown in figure 1-1. The output of a 38.4 KHz crystal oscillator timing source is fed into a divider chain. The divider chain provides signals with frequencies of 20 pulses per second, one pulse per second, and one pulse per minute. Finally, the one pulse per minute signal is fed into the Launch Counter. The latter provides the signals associated with events occurring immediately after launch. The figure also indicates the test chassis and digital difference detector circuitry used to test the redundant equipment.

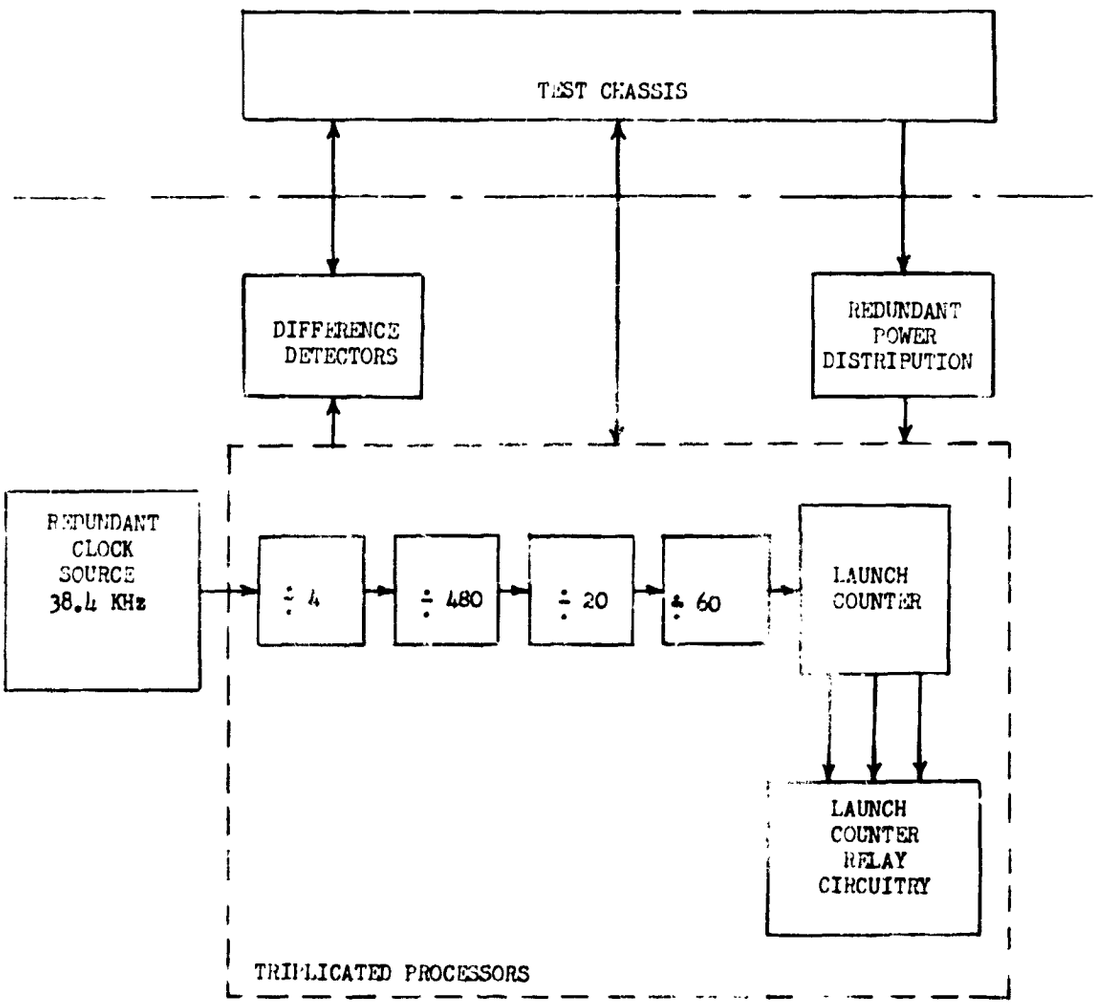

Figure 1-1. General Block Diagram, Redundant Sequencer Breadboard System

The model was constructed in accordance with the details of the previous design study. The primary redundancy technique employed is multiple-line majority voted logic. This technique requires the use of three replicas of each process appearing in the non-redundant version of the equipment. At selected locations, sets of majority voters (restorers) are inserted at the outputs of the replicated processors. The sets of voters compare equivalent signals and remove the effects of any minority of errors. The outputs of the majority voters are used as the replacements for the output signals from the associated processors.

In addition to the use of multiple-line logic, special circuits are utilized to satisfy requirements peculiar to the redundant system configuration. Among these are those required for providing a redundant clock source, testing the redundant equipment, maintaining synchronization between the multiple replicas, providing reliable power supplies, and maintaining high reliability at the interface between redundant and non-redundant subsystems.

In the following section (Section 2), the basic functions of the logic, test equipment and individual circuits are summarized. In the final section (Section 3), the details of the test program are presented along with a description of all system changes which have occurred since the writing of the Phase I report. A complete set of detailed system logic diagrams, schematic diagrams and parts lists are included in the appendices.

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2. System Description

2.1 Mechanical Configuration

The mechanical configuration for the breadboard system is shown in the frontispiece, figure 1-0. The sequencer chassis, shown on the right is a conventional 3 row card rack containing 3 in. x 4 in. printed circuit cards. All triplicated digital logic is implemented using printed circuit cards located within the card rack. All logic associated with one replica of the triplicated logic is located within a single card level. In addition to the multiple-line logic, the card rack also contains 7 digital difference detector cards, 1 flip-flop card, and 1 gate card used only for test purposes. These cards are located on the extreme right hand side of the card rack. The redundant clock source, regulators and power distribution circuitry are located on a panel attached to the back of the card rack.

The above configuration for the sequencer chassis provides maximum accessibility to the clock and power circuitry and also provides a high degree of accessibility to the multiple-line logic. Test points, located on each printed circuit card, allow monitoring of individual circuit outputs on the cards. Extender cards are supplied which allow individual printed circuit cards to be operated with their components completely accessible.

The test chassis, shown on the left in the photograph, contains all input-output controls and indicators required for the operation and test of the sequencer. In addition, the test chassis contains the DC power supplies required by the system. The test panel includes a system block diagram overlay so that all controls and indicators can be directly associated with their respective sections of the system.

2.2 Logical Design

A detailed block diagram of the triplicated sequencer system, showing all test controls and indicators is shown in figure 2-1, "Redundant Sequencer Block Diagram." The diagram indicates the interconnection of the three replicas of the counter chain at the majority voters. Note that feedback connections are provided from the voter outputs back to the processors in order to keep the triplicated processors synchronized.

The logic design consists primarily of the implementation of a series of counters for frequency division and the required decoding for output signals. The clock source and primary divider chain provide square wave outputs of 38.4 KHz and 9.6 KHz, and pulses at 20 per second, one per second, one per minute, and one per seven hours. The occurrence of the first seven hour pulse after clearing of the counters is adjustable with the update signal

to any one-hour interval. The update verify provides an output pulse for every update input pulse. The portion of the divider chain beyond the 1PPM output is called the Launch Counter. The Launch Counter decoding provides outputs at 1 pulse per hour, 1 pulse per 68 minutes, 1 pulse per 17 hours, and a special clear and counting signal which is set as a result of the clear input and is normally reset after the third count pulse to the Launch Counter. This signal is used to simulate Launch Clamp to inhibit setting any relays. The first 68 minute pulse occurs 56 counts after the Launch Counter is cleared and is used to set relay L-1. Relay L-2 is set by the 1 pulse per hour signal; relay L-3 is set by the 1 pulse per 17 hour signal; both L-1 and L-2 are set when L-3 is set.

The test circuitry indicated in the diagram includes the digital difference detectors, the processor and voter output forcing controls, the 20 times and 60 times speed-up controls and the output indicators. The digital difference detectors, which are located at each set of processor outputs and at each set of voter outputs, are test aids which detect and indicate any difference in the operation of the three replicas of the counter chain. The primary functions of the forcing controls are: 1) to provide a means of testing the difference detectors and 2) to force single rank operation of the system. Single rank operation is the normal method used to detect failures in the system which would be masked by the majority voters. A detailed discussion of single rank testing is included in section 3. The speed-up controls allow high speed operation, of the low speed counters at the end of the counter chain, to facilitate testing. Output indicators, driven by test flip-flops which toggle on each output pulse, are located at the 1PPM voter outputs, the update verify outputs and the 1 pulse/7 hour outputs. Indicator lights are also supplied for the clear and counting output and for each relay.

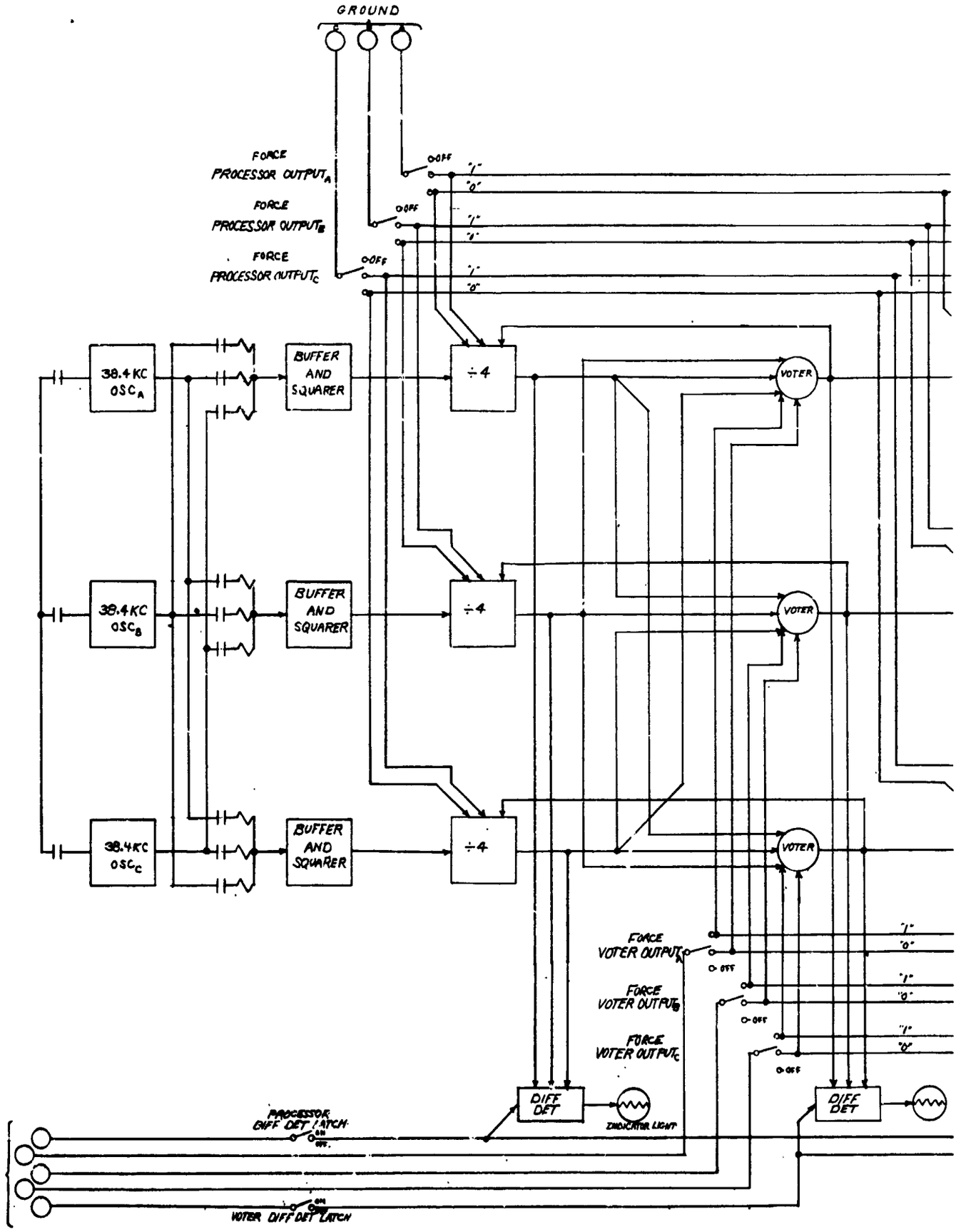
The detailed operation of the logic circuitry for each of the processors in the system is provided in the following paragraphs. Additional detail on the test circuitry is provided in section 2. 3.

2. 2. 1 Clock Source

The redundant crystal oscillator provides the clock source for the primary divider chain. It is shown in figure B-1 of the appendix and is described in section 2. 4.

2. 2. 2 Divide-by-4

The first counter divides the clock frequency by four, providing a 9.6 KHz square wave. The counter is a simple inverting shift register of two flip-flops, with a voter within the loop providing the restored output and in-line synchronization, as shown in figure 2-2. The actual logic diagram includes inverting gates to provide the processor forcing gate, the set and reset inputs to the first bit, and to drive the clock inputs on the next counter.


GROUND
FORCE PROCESSOR OUTPUT A
FORCE PROCESSOR OUTPUT B
FORCE PROCESSOR OUTPUT C
OFF
"1"
"0"
38.4 KC OSC A
38.4 KC OSC B
38.4 KC OSC C
BUFFER AND SQUARER
÷4
VOTER
FORCE VOTER OUTPUT A
FORCE VOTER OUTPUT B
FORCE VOTER OUTPUT C
DIFF DET
INDICATOR LIGHT
PROCESSOR DIFF DET LATCH
ON
OFF
VOTER DIFF DET LATCH
GROUND

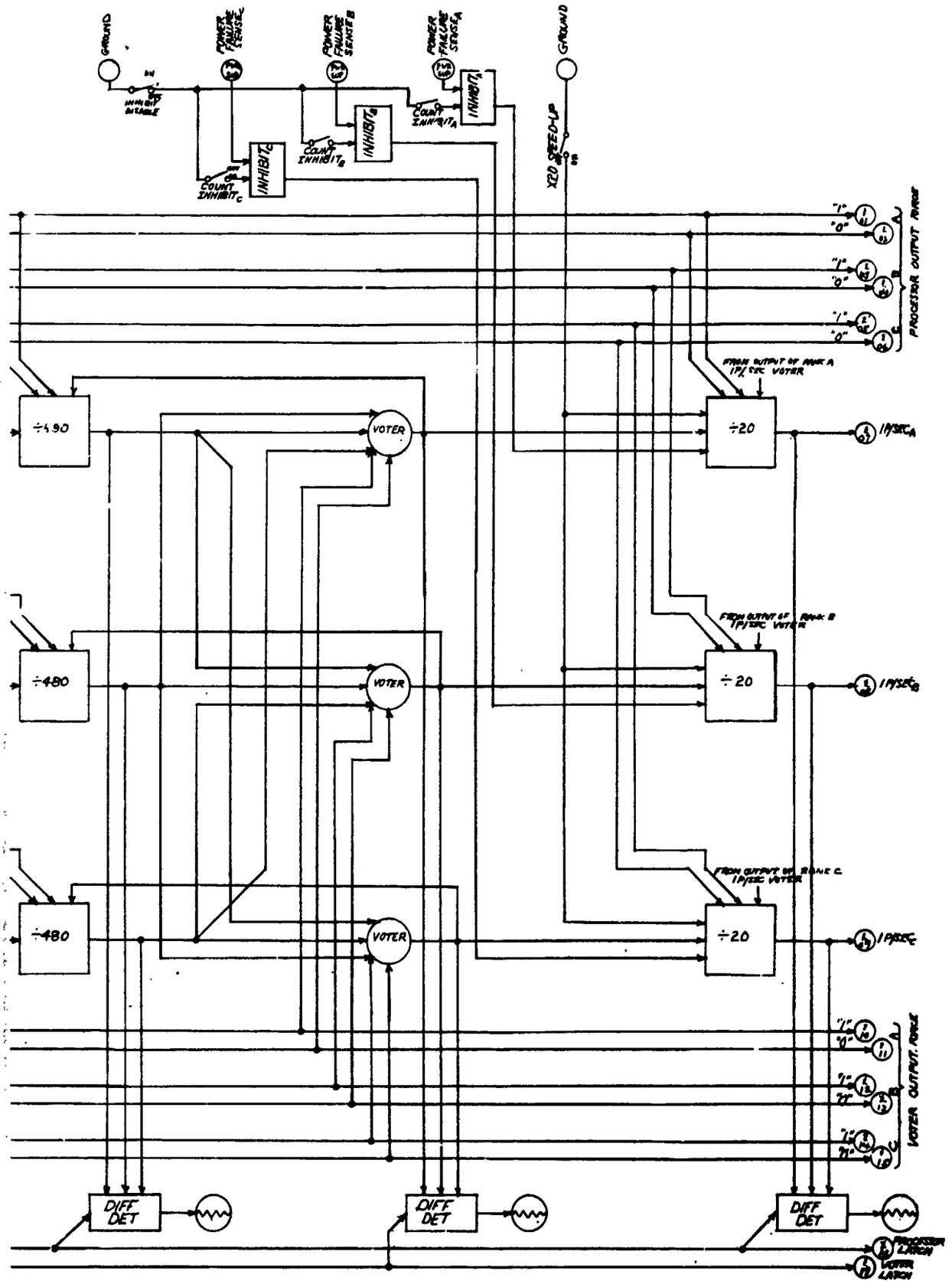
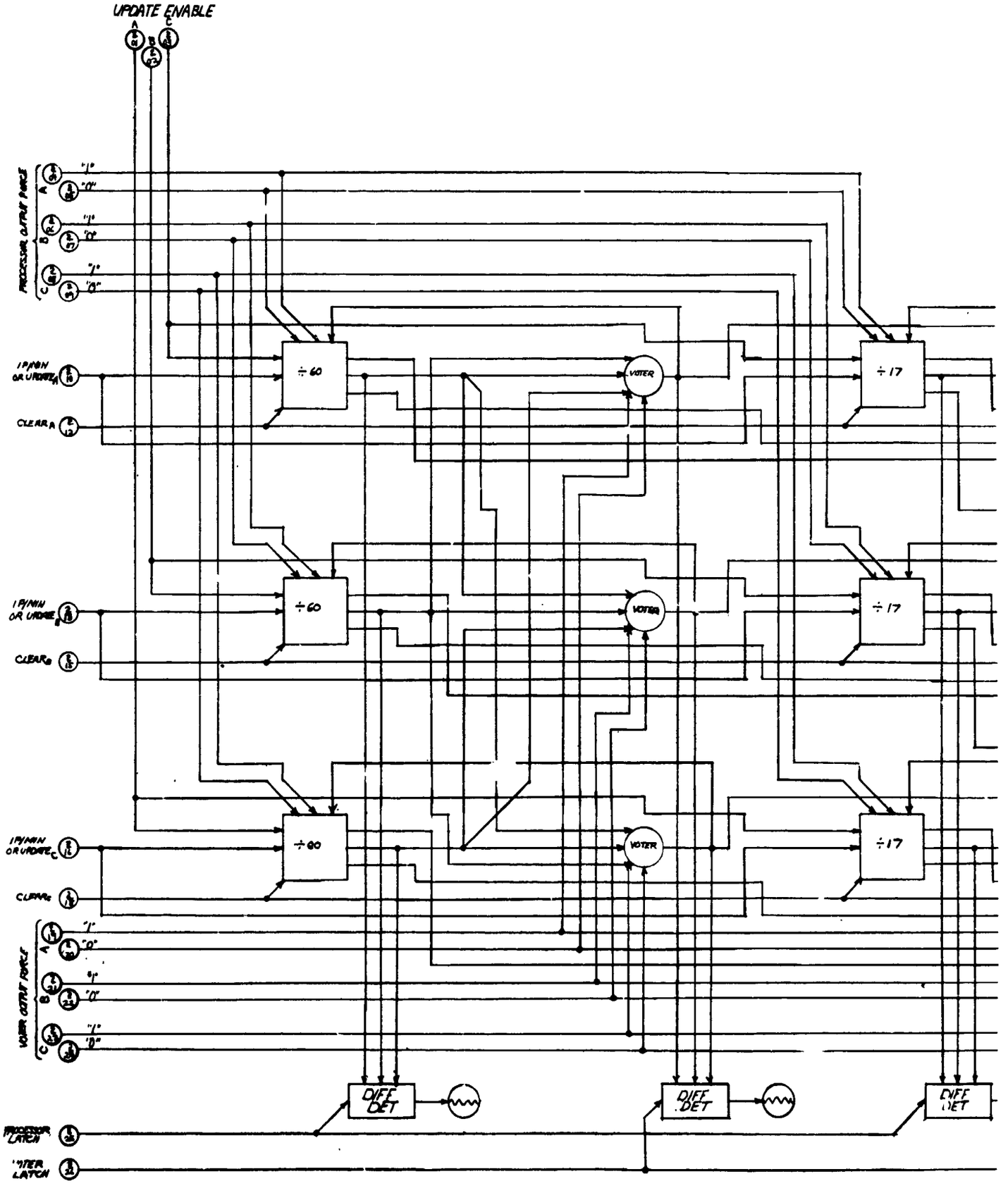


Figure 2-1. Redundant Sequencer Block Diagram (Sheet 1 of 4)


UPDATE ENABLE
A
B
C
PROCESSOR OUTPUT FORCE
A
B
C
"1"
"0"
"1"
"0"
"1"
"0"
I P/MIN OR UPDATE A
CLEAR A
I P/MIN OR UPDATE B
CLEAR B
I P/MIN OR UPDATE C
CLEAR C
VOTER OUTPUT FORCE
A
B
C
"1"
"0"
"1"
"0"
"1"
"0"
PROCESSOR LATCH
VOTER LATCH
÷ 60
÷ 60
÷ 60
VOTER
VOTER
VOTER
÷ 17
÷ 17
÷ 17
DIFF DET
DIFF DET
DIFF DET

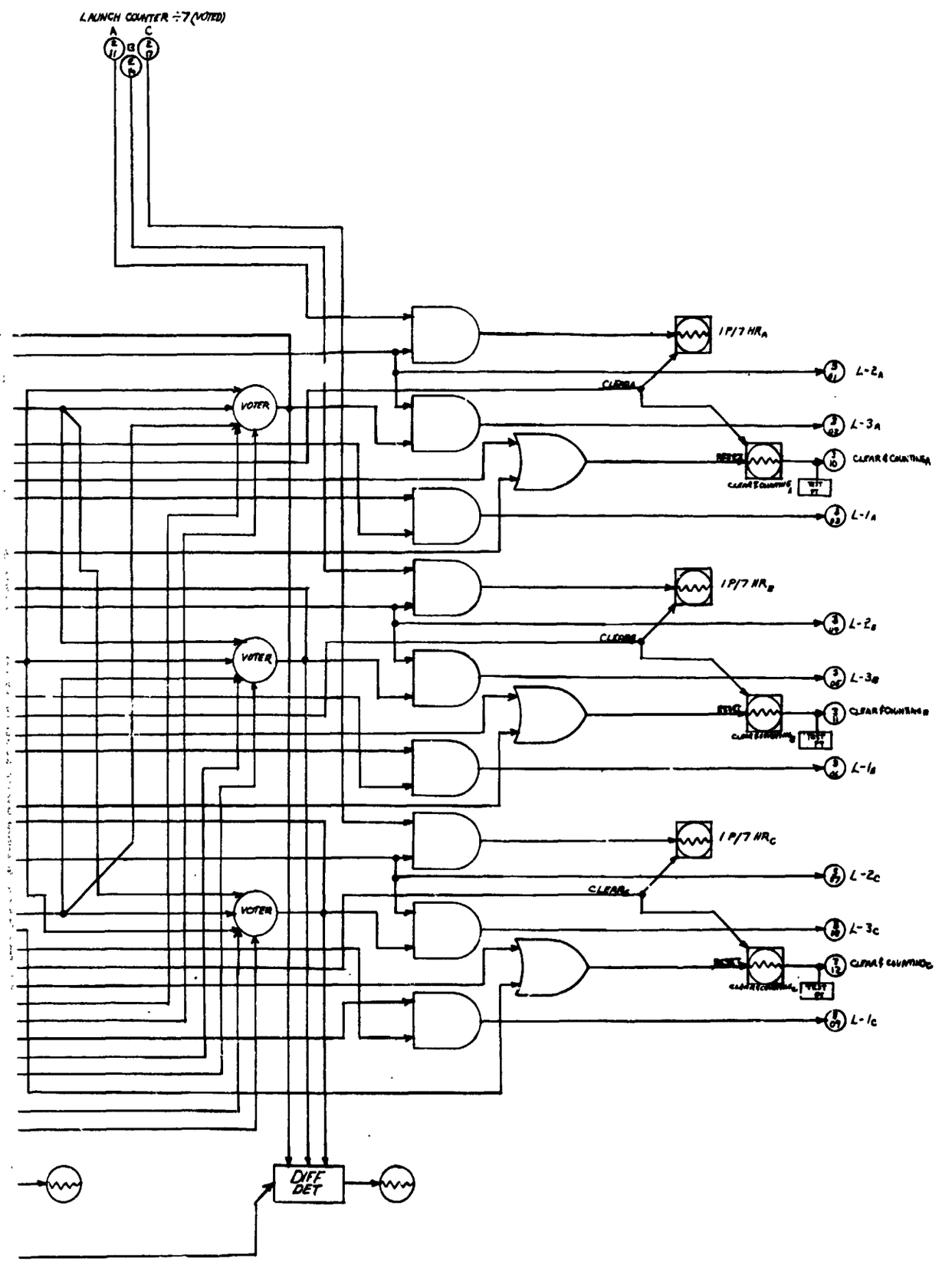
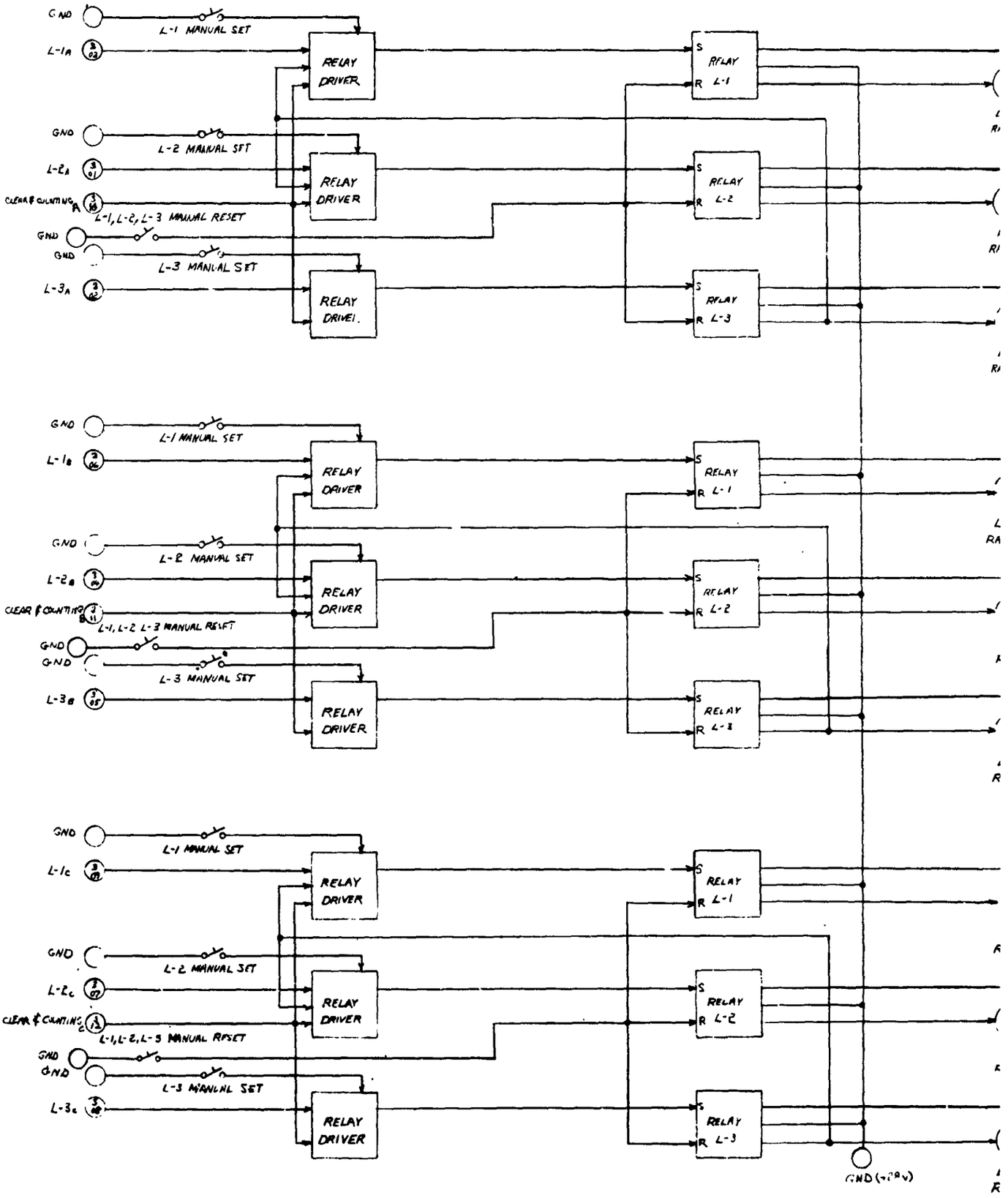


Figure 2-1. Redundant Sequencer Block Diagram (Sheet 3 of 4)

2-6


GND
L-1 MANUAL SET
L-1A
RELAY DRIVER
S
R
RELAY L-1
GND
L-2 MANUAL SET
L-2A
RELAY DRIVER
RELAY L-2
CLEAR & COUNTING A
L-1, L-2, L-3 MANUAL RESET
GND
GND
L-3 MANUAL SET
L-3A
RELAY DRIVER
RELAY L-3
GND
L-1 MANUAL SET
L-1B
RELAY DRIVER
RELAY L-1
GND
L-2 MANUAL SET
L-2B
RELAY DRIVER
RELAY L-2
CLEAR & COUNTING B
L-1, L-2 L-3 MANUAL RESET
GND
GND
L-3 MANUAL SET
L-3B
RELAY DRIVER
RELAY L-3
GND
L-1 MANUAL SET
L-1C
RELAY DRIVER
RELAY L-1
GND
L-2 MANUAL SET
L-2C
RELAY DRIVER
RELAY L-2
CLEAR & COUNTING C
L-1, L-2, L-3 MANUAL RESET
GND
GND
L-3 MANUAL SET
L-3C
RELAY DRIVER
RELAY L-3
GND (+28V)

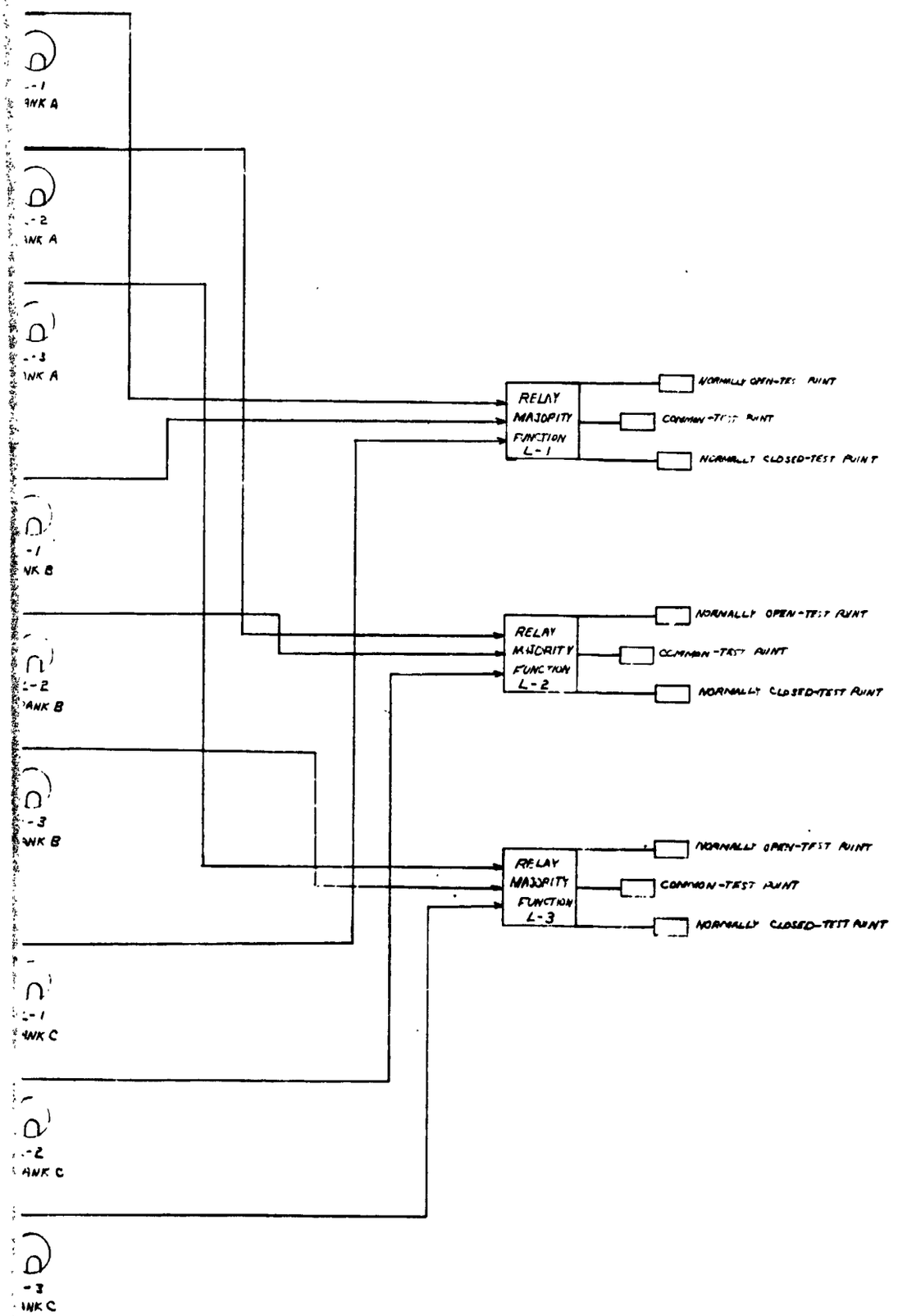
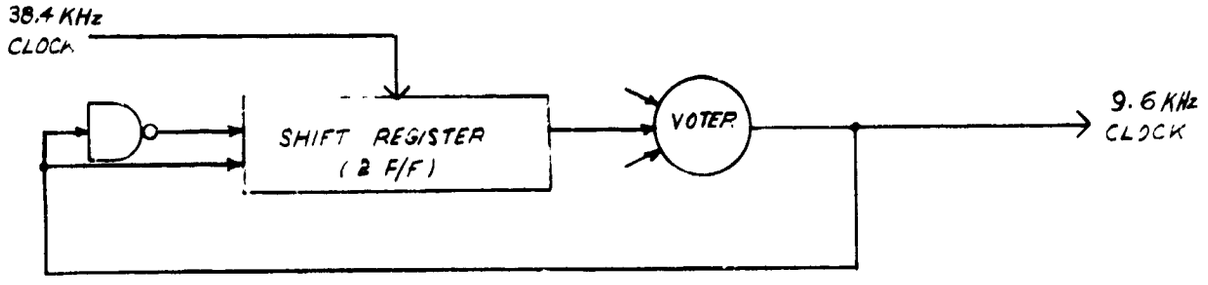


Figure 2-1. Redundant Sequencer Block Diagram (Sheet 4 of 4)



(INVERTING RING COUNTER)

COUNTER SEQUENCE

Count	1	2	Output
0	0	0	0
1	1	0	0
2	1	1	1
3	0	1	1
0	0	0	0

Figure 2-2. Divide-by-4 Counter Block Diagram

2.2.3 Divide-by-480

The second counter divides the 9.6 KHz clock by 480, providing a "0" output pulse once for every 480 input clock pulses. This counter is shown in figure 2-3. It is implemented with a 512 state key stream generator, or linear feedback shift register, of 6 bits. All 512 states may be generated by altering the feedback so that the all 0's state, not in the normal sequence, is included as a state in the full sequence. Although this counter is modified to provide only a 480 state sequence, the all 0's state is included in the complete sequence to insure that the redundant counters may always be synchronized with the reset signal. This reset is generated from the majority voted output clock pulse, because there are no synchronizing voters within the feedback loop. In the event that one register reaches state 480, but there is no synchronizing reset, it will continue counting through the remainder of the full sequence but will remain in the all 0's state until the synchronizing reset inserts the initial state in all counters. The 0's state is also decoded as an output so that a majority output is always generated as soon as one other counter generates an output. As described for the divide-by-4, the actual logic diagram includes additional gates required for inversion and additional diodes for expanding fan-in capability and to provide the processor forcing input.

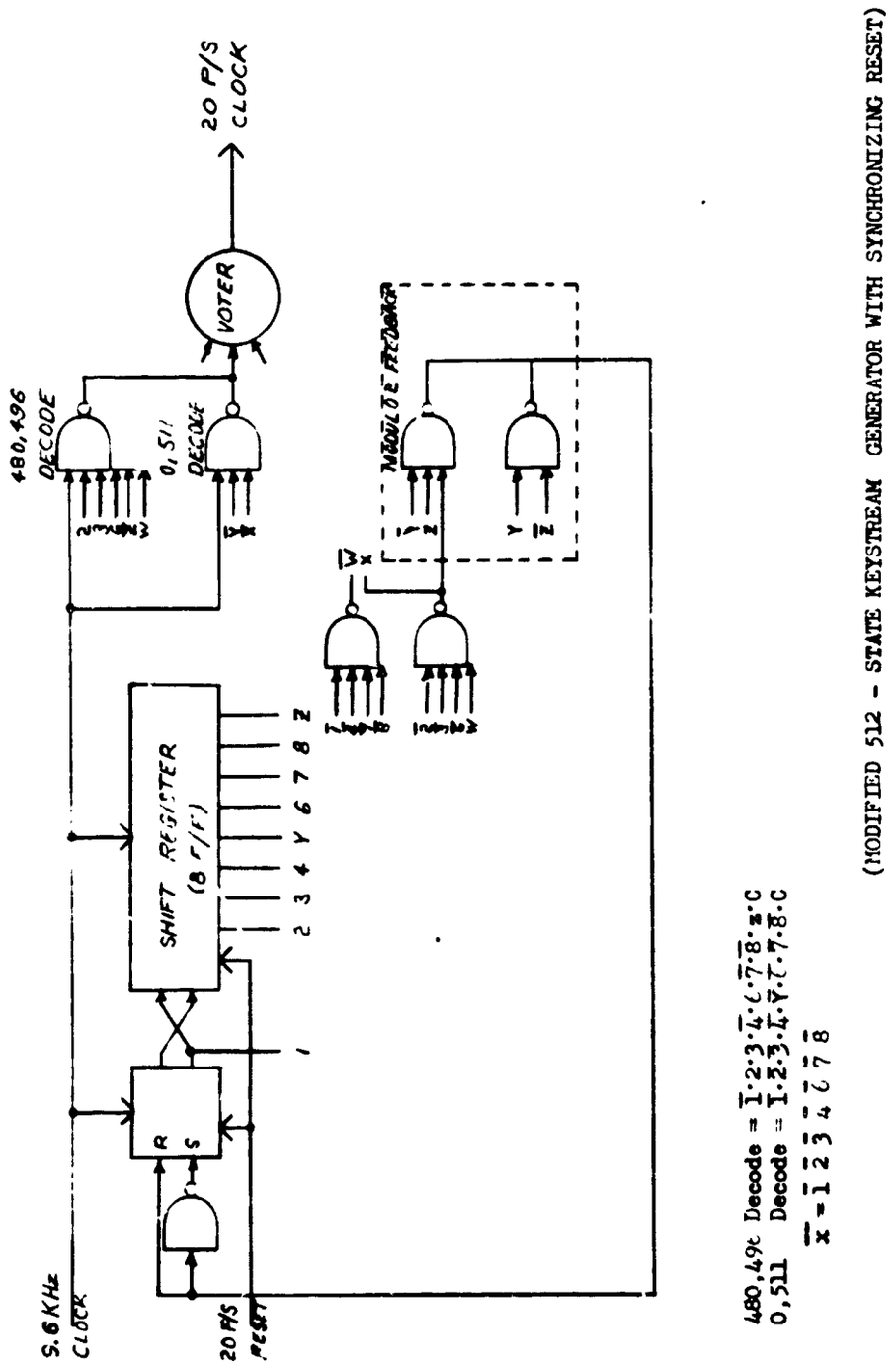


Figure 2-3. Divide-by-480 Counter Block Diagram

The set and reset sides of the first flip-flop in the register are redefined to permit the use of the synchronizing reset to set the first bit and reset all remaining bits, using the common DC reset input available on the standard logic card.

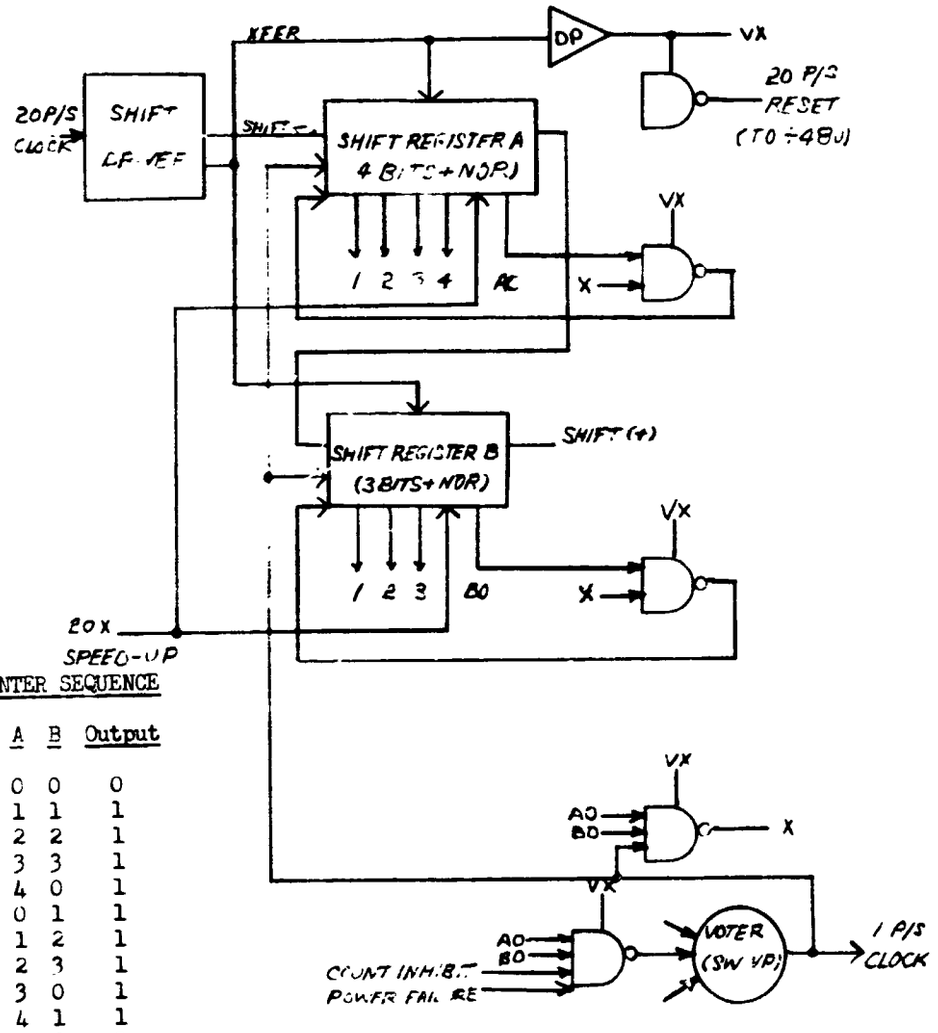
The logic signals are indicated in symbolic form, and are defined as follows: The output of the register bits are numbered consecutively in the direction of shifting, with bit 1 referred to as the first, or least-significant bit (least numbered, not least weighted). The two bits required as inputs to the modulo-2 feedback are not designated with the appropriate number, but are symbollically designated to clearly identify these signals. The last, or most significant bit is necessarily an input to the modulo-2 feedback and is designated z. The other input is designated y; for this particular counter it is the fifth bit. The signal designated x is the special signal which is a ground only if the counter has proceeded past the normal decoded output without being reset. In this case, the x signal inhibits the feedback otherwise generated by the modulo-2 feedback when the counter reaches the state where all bits except the last are 0. This forces the counter to the all 0's state after the next clock pulse; it remains in the all 0's state and generates an output pulse for every clock pulse until the synchronizing reset is applied to begin a new counting cycle. In normal operation, neither the x signal nor the all 0's decode should ever be "ON", because they are active only when the counters are out of synchronism.

The signal designated w has no special significance, except that it is a convenient factoring of terms common to both the output decode and the x signal.

2.2.4 Divide-by-20

The third counter divides the 20 PPS clock by 20, and provides a "0" output pulse of fixed duration (approx. 6.5 μsec) after each 20 input clock pulses. In addition, this counter provides the feedback synchronizing reset pulse, also of approximately 6.5 μsec duration, after every input clock pulse. The 1 PPS clock output may also provide an output for every input clock pulse when a ground is applied to the 20X speedup input. A ground applied to either the count inhibit or power failure inputs will prevent the occurrence of any output clock pulses. The divide-by-20 counter is shown in figure 2-4.

The divide-by-20 counter is the highest frequency magnetic counter. The shift driver is a monostable circuit which is activated by the trailing edge (the positive-going edge of the grounding 20 PPS clock pulse) of the input pulse. It remains active for a fixed period of time (approx. 6.5 μsec.) after which it returns to the quiescent state, where no significant power consumption is required until the next input clock pulse. The state of the counter is stored in the non-volatile magnetic shift registers, and is available for logic decoding only during



COUNTER SEQUENCE

Count	A	B	Output
0	0	0	0
1	1	1	1
2	2	2	1
3	3	3	1
4	4	0	1
5	0	1	1
6	1	2	1
7	2	3	1
8	3	0	1
9	4	1	1
10	0	2	1
11	1	2	1
12	2	0	1
13	3	1	1
14	4	2	1
15	0	3	1
16	1	0	1
17	2	1	1
18	3	2	1
19	4	3	1
0	0	0	0

(INCLUDING 20 x SPEED-UP, COUNT INHIBIT AND
20P/S RESET FOR DIVIDE BY 480 SYNCHRONIZATION)
(4x5 Mixed Base Modulo Counter)

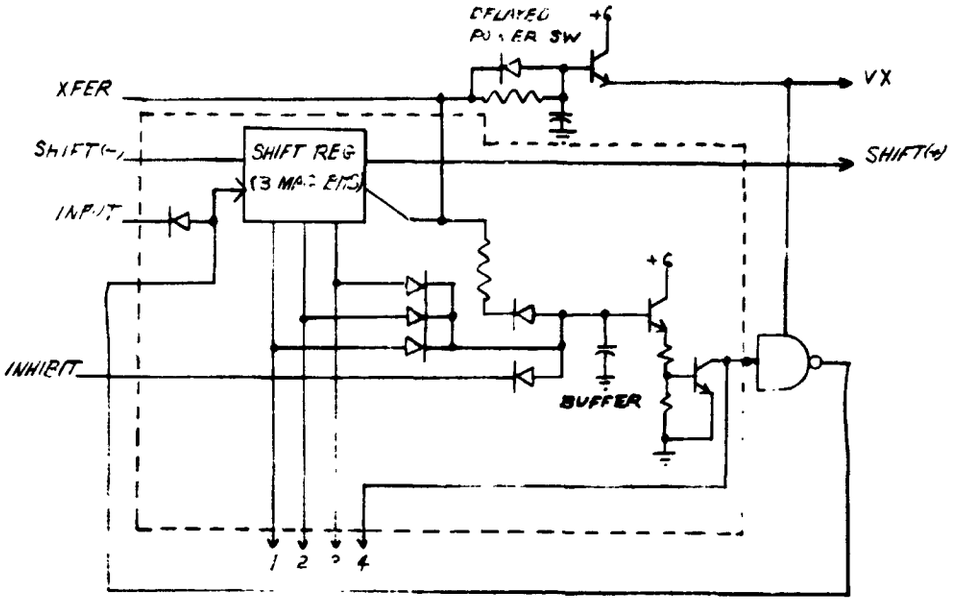
Figure 2-4. Divide-by-20 Counter Block Diagram

the time that the shift driver is active. Because it is necessary that both the output decode and the feedback synchronizing reset gates have a signal that indicates that the shift driver is active, and no gating of any kind is required when the shift driver is inactive, the power to all gates is switched on only during the time that the shift driver is active. This results in no power consumption required for logic gates or information storage. In addition, because there is no need for majority voting when all corresponding shift drivers in each replica are not active, power is switched on for the voters only when at least one corresponding shift driver is active. Further more, all the associated circuitry, such as the buffers and OR gates, the power switches, as well as the shift driver itself require no power when the shift driver is inactive. Therefore, no stand-by power, and very low average power, is required for all of the magnetic logic due to the low duty cycle required.

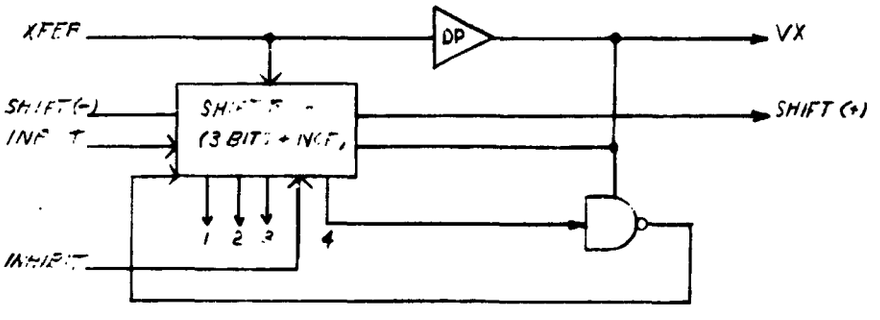
The logic for the ring counters used in the divide-by-20 counter is shown in symbolic form, as illustrated in figure 2-5, which also shows the more detailed version of the typical ring counter. This diagram shows that the number of magnetic bits is actually less than the length of the ring counter, and that the last bit is decoded as the NOR of the output of the magnetic bits. This configuration insures that the output from each ring is unique (i.e., occurs only once each cycle), and allows resynchronization by simply inserting a 1 in the first bit.

The divide-by-20 counter consists simply of two ring counters whose lengths are relatively prime (contain no common factors). Both shift registers are driven by the shift driver: however, the position of one register precesses with respect to the other so that they return to the same relative position only once every 20 input clock pulses.

The divide-by-20 counter is synchronized by inserting a 1 in the first bit of both ring counters whenever a majority voted clock output pulse is generated. The signal designated x is active only if the counter is in the state where the counter output pulse would be generated, but there is no majority voted output pulse. Since the counter output pulse is generated only when all 1 of the magnetic bits are reset, the x signal will force the counters to remain in this state and generate an output pulse for every clock input until a majority voted output pulse is generated to synchronize all counters. The synchronizing input is also connected to the buffer inhibit input, so that any magnetic register outputs which may have occurred at that time will be eliminated. The x signal is not active during normal counter operation; however, the application of the count inhibit or the power failure inhibit will cause the x signal to become active after the counters reach the output state, because the output to the majority voters is inhibited.



TYPICAL RING COUNTER
(Shown for a 4-Bit Counter)



BLOCK DIAGRAM

Figure 2-5. Typical Synchronizing Ring Counter

2.2.5 Divide-by-60

The next counter is the divide-by-60 counter, shown in figure 2-6. It is a modified 64-state KSG, very similar to the divide-by-480 counter, with the following variations:

a. The register contains 6 magnetic bits, with 64 possible states; both state 60 and the all 0's state are decoded in a single gate by deleting the one input that differs between the two states.

b. The synchronizing reset is driven by a set driver which provides the longer pulse width necessary to set the initial state into the magnetic shift register.

c. All gates and the voter are driven by the appropriate power switch, so that no stand-by power is required.

d. The 60X speedup is a ground signal applied to the inhibit input of all buffers which provide inputs to the output decode. This forces the counter to generate an output pulse after every input clock pulse, and prevents any bits in the shift register from proceeding down the register.

e. The clear input (not shown on the functional diagram) inserts the all 0's state so that an output pulse is generated after the first input clock pulse after being cleared.

2.2.6 Launch Counter

The Launch Counter uses mixed base ring counters similar to the divide-by-20 counter, although the configuration is more complex, as shown in figure 2-7. The Launch Counter also contains output decoding for the Launch event timing and the clear and counting indicator, and provides the update function and the update verify output. The W, X, and Y registers form the divide-by-60 portion which operates with output resynchronization in a nearly identical manner to the divide-by-20 counter, except that update enable, designated by E, can prevent the insertion of the first bit of the ring counters. Both the V register (7 bits) and the Z register (17 bits) have voters within the feedback loop, so no other resynchronizing is necessary or desirable.

The Z register differs from the other ring counters by a few minor changes. The NOR output of the 16 magnetic bits is not generated with one gate and buffer combination, but is instead split into the even and odd numbered bits. The buffer output for the even bits, designated Z0(E), is a 0 whenever an even-number state (2 through 16, but not zero) is read out of the register. Likewise, the buffer output designated Z0(O) is a 0 whenever any of the odd-numbered states (1 through 15) is read out, neither buffer is a 0 for the 0 state readout.

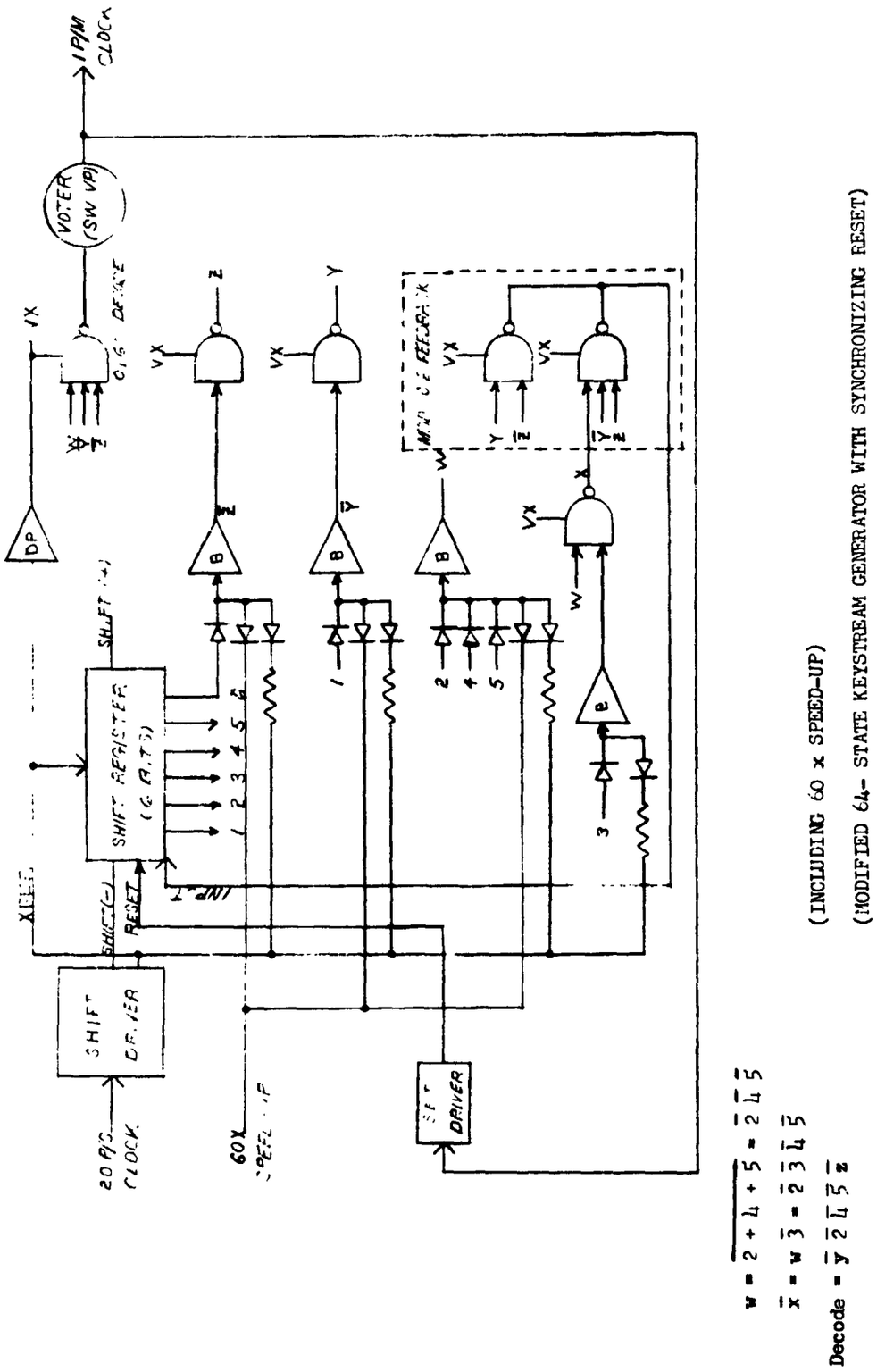


Figure 2-6. Divide-by-60 Counter Block Diagram

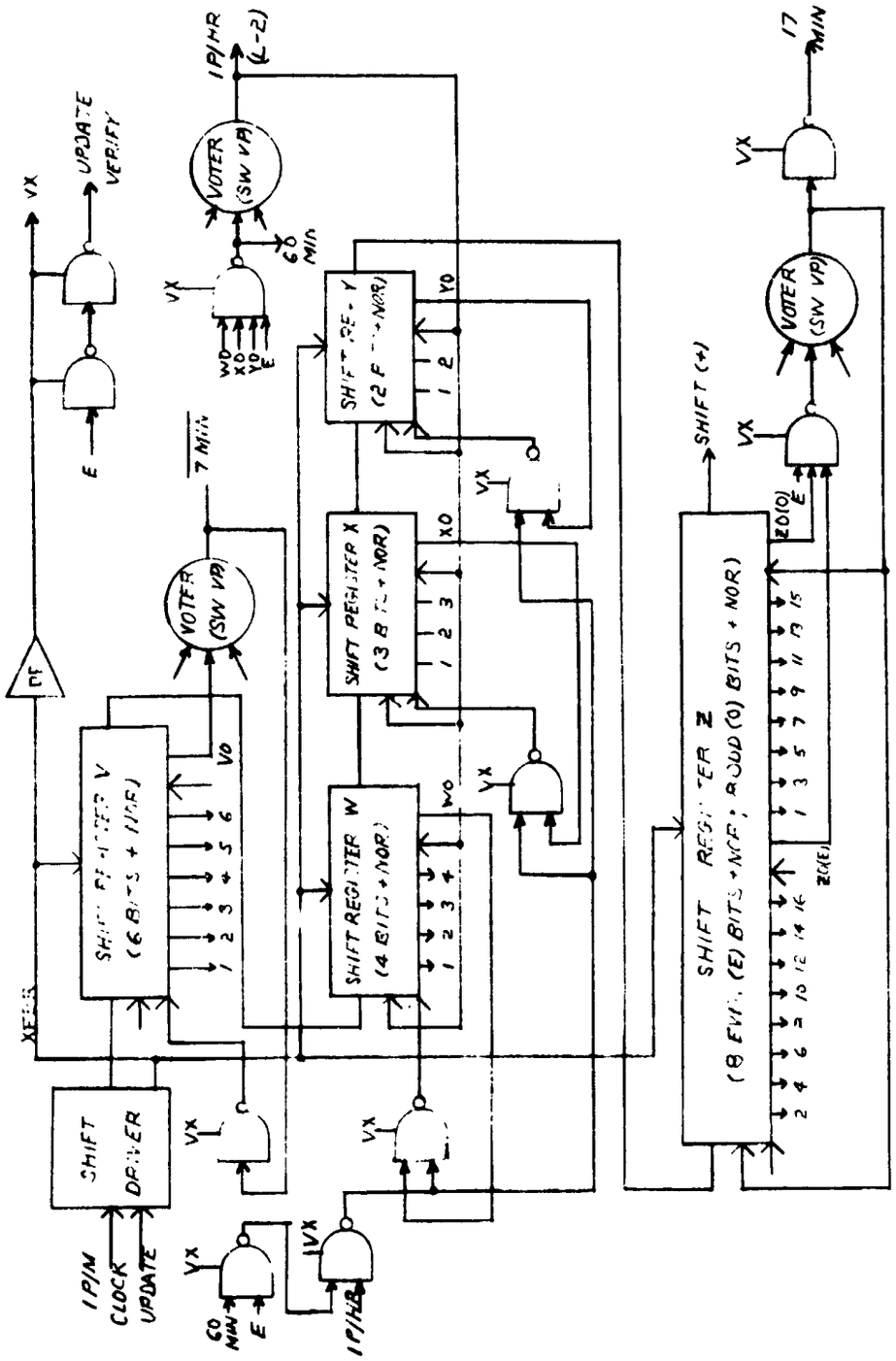


Figure 2-7. Launch Counter Block Diagram (Sheet 1 of 2)

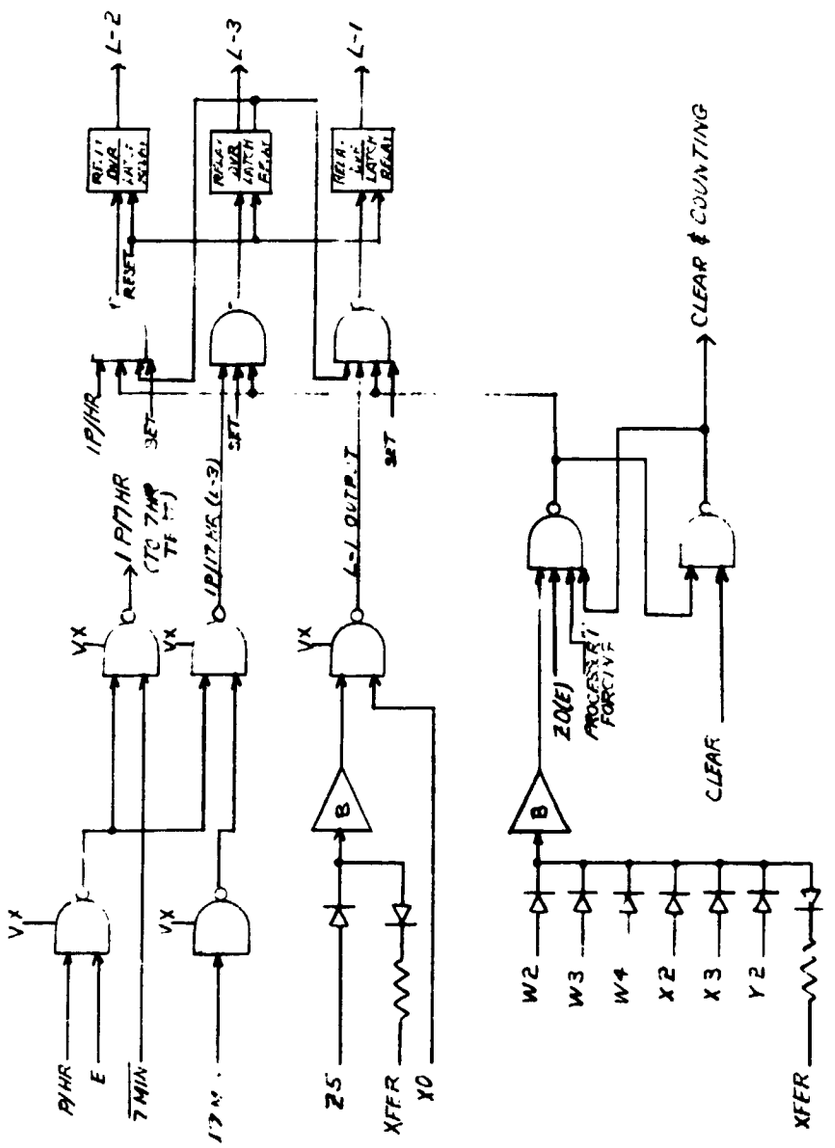


Figure 2-7. Launch Counter Block Diagram (Sheet 2 of 2)

Since the register begins with the readout of the 0 state after the first clock pulse after being cleared, and proceeds in normal counting sequence through the remaining states to 16 and back to 0, Z0(E) is a 0 every other clock pulse, except for states 0 and 1. It is this characteristic of Z0(E) which allows it to be used as a reset input to the clear and counting flip-flop. The clear and counting flip-flop is also reset by any of the states of the W, X, and Y registers except the 0 state and the 1 state. This means that the clear and counting will always be reset by the first or second clock pulse input to the Launch Counter, unless all of the W, X, Y, and Z registers have been cleared. Only in this case will the clear and counting flip-flop remain set until the third clock pulse input to the Launch Counter.

The Z register is also prevented from recirculating when a ground is applied on the Update Enable (designated E) input. This means that neither the W, X, Y, or Z registers will count during Update Enable if they were previously cleared, so that the clear and counting flip-flop should remain set during the update procedure, regardless of the number of clock pulse inputs. In order to permit resetting of the clear and counting flip-flop from the test panel, the signal which forces the processor outputs to 1 will also reset the clear and counting flip-flop. The feedback input to the first bit of the Z register uses the diode isolated input to permit the use of voter pullups.

The launch event timing is decoded from the W, X, Y and Z registers. L-1 is decoded from state 5 of the Z register and state 0 of the X register, resulting in an output 56 minutes after the first clock pulse input after clearing, and every 68 minutes thereafter, because 56 mod 17=5, 56 mod 4=0, and 17x4=68. L-2 is taken directly from the 1 PPHR signal, resulting in an output after the first clock pulse input and every 60 thereafter. L-3 is decoded as state 0 of W, X, Y, and Z, resulting in an output after the first clock pulse and every 17 hours thereafter. L-1 and L-2 may also be set by L-3, and all 3 events may be set by the common launch clamp which is simulated by the clear and counting flip-flop, or the individual manual set inputs. Although not so indicated on the block diagram, the individual manual set inputs and the launch clamp inputs are more directly coupled, so that they may cause a relay to set even though either of the other logic inputs is already applied. The manual reset input is directly coupled and overrides any of the set inputs.

Except for the common clear and shift driver input, the V shift register (7 bits) operates independently from the remainder of the Launch Counter. It is always stepped by the shift driver, regardless of the Update Enable, and does not enter into any of the launch event decoding. It can therefore be preset to any state prior to the actual Launch Counter counting. The position of the V register when the remainder of the Launch Counter begins counting determines which of the 1 PPHR outputs will coincide with the first 7 min. output to generate

the first 1PP 7 HR output. Since the V register advances a net of 4 positions for each 1PPHR output (60 mod 7=4), the number of update pulses must effectively increment the register 4 positions for each individual one hour or preset. Each exact multiple of 7, however, will result in a 1PP 7 HR output, which corresponds to a 7 hour preset. Therefore, the V register is advanced to the position which corresponds to the final position after 4 times the number of hours of preset desired. Since the position corresponds to the number of update pulses, the number is determined as 4N mod 7.

If the total preset desired is a multiple of 7, then the number of update pulses is exactly the same as the preset in hours. The number of preset hours in excess of multiples of 7 determine the number of additional update pulses as described above. These results are summarized below:

Preset 7M + N	Update 7M + 4N Mod 7
7M + 0	7M + 0
7M + 1	7M + 4
7M + 2	7M + 1
7M + 3	7M + 5
7M + 4	7M + 2
7M + 5	7M + 6
7M + 6	7M + 3

2.3 Test Equipment Design

2.3.1 Test Logic

The test equipment, supplied with the sequencer breadboard, includes:

1) Test logic, located in the sequencer chassis, which assists in the monitoring and testing of the sequencer.

2) The test chassis, which provides the input controls and output indicators necessary for the operation and test of the sequencer chassis.

The test logic, shown in figure A-8 of Appendix A includes the digital difference detectors and indicator light driving circuits. The electrical location of the digital difference detectors, at the outputs of processors and voters, is shown in figure 2-1. The operation of the difference detector circuit is covered in section 2.4.7. The primary function of the difference detector circuits is to assist in the location of failures that cause output errors in the system. The difference detectors can be operated in a latching mode so that temporary differences

will be indicated. The 1PPM, update verify and 1 P/7 HR indicator lights are driven via flip-flops which toggle on each output pulse. The toggle flip-flops are included because the normal 6.5 μsec output pulses would not be sufficient to light the indicator lights. All indicator lights except the relay lights are driven by isolating NAND gates to prevent cross-talk in the test cable from affecting output signals. Note that the nine test logic cards can be removed from the sequencer chassis without affecting the operation of the sequencer. Note also that if the difference detector cards are removed, all processor and voter forcing lines are broken thus eliminating the possibility that a failure on the forcing line will cause failure of a complete replica.

2.3.2 Test Chassis

The test chassis front panel is shown in figure A-12 of Appendix A, and the test chassis diagram is shown in figure A-9 of Appendix A.

The test panel contains a block diagram of the sequencer, on which the test input switches and output lights are located. In addition to the inputs and outputs normally required by the sequencer for operation, the test panel contains the difference detector indicators and forcing switches required to check for and locate internal failures which would be masked by the triple redundancy. Difference detector indicators are located at the outputs of each voter and processing unit. A voter and a processor forcing switch is provided for each replica.

The difference detector indicators are activated by any significant differences between outputs of corresponding processors and voters in the triplicated system. The difference detector indicators operate in two modes, latching and non-latching, as determined by the difference detector latch switches.

The forcing switches allow the operator to force all processor and/or voter outputs in a given replica to "one" or "zero." This capability allows the operator to test replicas, voters and difference detectors. Thus, to test replica C the processor outputs of replica A are forced to be different than the processor outputs of replica B. Replica C then determines the voter outputs. The combination of difference detectors and single rank testing provides the operator with a convenient method of detecting and locating all failures in the triplicated system.

In addition to the controls and indicators, the test chassis contains the D. C. power supplies for the breadboard system, as indicated in the test chassis diagram.

A complete listing and description of test chassis controls and indicators is given below:

1) Test Panel Switches

S-1 Processor Difference Detector Latch (determines whether Processor Difference Detector Lights will be latched on after one difference detection or will be free to go ON and OFF, providing an instantaneous indication).

S-2 Processor Forcing Switch, Rank A (forces a constant logical 1 or 0 output on all replica Counters; is off in normal operation).

S-3 Processor Forcing Switch, Rank B (similar to S-2).

S-4 Processor Forcing Switch, Rank C (similar to S-2).

S-5 Voter Difference Detector Latch (similar to S-1).

S-6 Voter Forcing Switch Rank A (forces a constant logical 1 or 0 output on all replica A Majority Voters; is off in normal operation).

S-7 Voter Forcing Switch, Rank B (similar to S-6).

S-8 Voter Forcing Switch, Rank C (similar to S-6).

S-9 Count Inhibit, Rank A (inhibits the replica A÷20 Counter stopping all following replica A counters if the Inhibit Disable switch is in the off position).

S-10 Count Inhibit, Rank B (similar to S-9).

S-11 Count Inhibit, Rank C (similar to S-9).

S-12 X20 Speed-up (effectively by-passes ÷20 Counter in all replicas).

S-13 Clear, Rank A (clears first ÷60 and all following replica A counters).

S-14 Clear, Rank B (similar to S-13).

S-15 Clear, Rank C (similar to S-13).

S-16 X60 Speed-up (effectively by-passes first ÷60 Counter in all replicas).

S-17 Update, Rank A (provides one-shot pulse to replica A Launch Counter, simulating normal Launch Counter input signal).

S-18 Update, Rank B (similar to S-17).

S-19 Update, Rank C (similar to S-17).

S-20 Update Enable, Rank A (inhibits ÷17 and second ÷60 Counters in replica A; for use when Up-dating ÷7 Counter).

S-21 Update Enable, Rank B (similar to S-20).

S-22 Update Enable, Rank C (similar to S-20).

S-23 Set L-1 Relay, Rank A (sets replica A L-1 Relay).

S-24 Set L-1 Relay, Rank B (similar to S-23).

S-25 Set L-1 Relay, Rank C (similar to S-23).

S-26 Reset Relays, Rank A (resets all replica A Relays).

S-27 Set L-2 Relay, Rank A (sets replica A L-2 Relay).

S-28 Set L-2 Relay, Rank B (similar to S-27).

S-29 Set L-2 Relay, Rank C (similar to S-27).

S-30 Reset Relays, Rank B (similar to S-26).

S-31 Set L-3 Relay, Rank A (sets L-3 Relay in replica A).

S-32 Set L-3 Relay, Rank B (similar to S-31).

S-33 Set L-3 Relay, Rank C (similar to S-31).

S-34 Reset Relays, Rank C (similar to S-26).

S-35 A.C. Power (a-c power switch for all d-c supplies).

S-36 28v D.C., Rank A (connects 28v input of replica A to 28v supply or to Test Chassis test point).

S-37 28v D.C., Rank B (similar to S-36).

S-38 28v D.C., Rank C (similar to S-36).

S-39 12v D.C., Rank A (connects 12v input of replica A to 12v supply or to Test Chassis test point).

S-40 12v D.C., Rank B (similar to S-39).

S-41 12v D.C., Rank C (similar to S-39).

S-42 8v D.C. (connects Power Sense input node of all Power Failure Detectors to unregulated d-c supply or to Test Chassis test point).

S-43 8v D.C. (identical to S-42).

S-44 Inhibit Disable (controls the Count Inhibit switches S-9, S-10 and S-11; if the three Count Inhibit switches are in the inhibit position, the Inhibit Disable switch serves as a master inhibit control for all the replicas by releasing the Count-Inhibits simultaneously).

2) Test Panel Lights

DS-1 ÷4 Counter (turned on by Difference Detector Circuits, indicating difference in output between ÷4 Counters; can give instantaneous indication or be latched on by first difference detection).

DS-2 ÷4 Voters (turned on by Difference Detector Circuits, indicating lack of agreement of any ÷4 Majority Voters; can give instantaneous indication or be latched on by first difference detection).

DS-3 ÷480 Counters (similar to DS-1).

DS-4 ÷480 Voters (similar to DS-2).

DS-5 ÷20 Counters (similar to DS-1).

DS-6 ÷20 Voters (similar to DS-2).

DS-7 ÷60 Counters (similar to DS-1, for first ÷60 Counters).

DS-8 ÷60 Voters (similar to DS-2, for first ÷60 Voters).

DS-9 1PPM, Rank A Voters (toggles at rate determined by output of first ÷60 Majority Voter in replica A, providing visual indication of replica operation; turned off by Clear S-12).

DS-10 1PPM, Rank B Voters (similar to DS-9; turned off by Clear S-13).

DS-11 1PPM, Rank C Voters (similar to DS-9; turned off by Clear S-14).

DS-12 ÷7 Counters (similar to DS-1).

DS-13 ÷7 Voters (similar to DS-2).

DS-14 ÷60 Counters (similar to DS-1, for second ÷60 Counters).

DS-15 ÷60 Voters (similar to DS-2, for second ÷60 Voters).

DS-16 ÷17 Counters (similar to DS-1).

DS-17 ÷17 Voters (similar to DS-2).

DS-18 Up-Date Verify, Rank A (toggles at rate determined by the replica A Launch Counter input signal when Up-Date Enable S-19 is in Enable position).

DS-19 Up-Date Verify, Rank B (similar to DS-18 with S-20).

DS-20 Up-Date Verify, Rank C (similar to DS-18 with S-21).

DS-21 1P/7 Hr., Rank A (toggles at rate determined by replica A Launch Counter).

DS-22 Clear and Counting, Rank A (turned off by replica A Launch Counter exactly two minutes after counting has begun provided all Counters were cleared prior to starting the sequence and all Counters function properly; or turned off by Rank A Processor 1 Forcing S-2 turned on by Clear S-12).

DS-23 1P/7 Hr., Rank B (similar to DS-21).

DS-24 Clear and Counting, Rank B (similar to DS-22; turned off by S-3, on by S-13).

DS-25 1P/7 Hr., Rank C (similar to DS-21).

DS-26 Clear and Counting, Rank C (similar to DS-22; turned off by S-4, on by S-14).

DS-27 L-1 Relay, Rank A (turned on by setting of replica A L-1 Relay).

DS-28 L-2 Relay, Rank A (turned on by setting of replica A L-2 Relay).

DS-29 L-3 Relay, Rank A (turned on by setting of replica A L-3 Relay).

DS-30 L-1 Relay, Rank B (similar to DS-27).

DS-31 L-2 Relay, Rank B (similar to DS-28).

DS-32 L-3 Relay, Rank B (similar to DS-29).

DS-33 L-1 Relay, Rank C (similar to DS-27).

DS-34 L-2 Relay, Rank C (similar to DS-28).

DS-35 L-3 Relay, Rank C (similar to DS-29).

DS-36 Power (turned on with a-c power).

2.4 Circuit Design

2.4.1 38.4 KHz Clock

The 38.4 KHz clock source employed in the sequencer is shown in the non-redundant sketch in figure B-1, Appendix B. The oscillator circuit is basically the NAVWEPS 16-1-519-2 Preferred Circuit PSC 31 with some modifications to meet the requirements of the redundant version. The circuit is recommended for crystal oscillators in the 20 to 100 KHz range. The oscillator is an amplified feedback type in which the feedback path is from the collector of Q2 to the base of Q1 through the crystal. The impedance of the crystal at series resonance is low enough to permit feedback of sufficient amplitude to start and maintain oscillations over the temperature range. The output signal from the oscillator at the collector of Q2 is a square wave with a good drive capability. The oscillator outputs are summed for each of the three replicas in the system and the load is driven via a buffer and squaring circuit. The oscillators are synchronized to each other via capacitors which connect the bases of the Q1 transistors.

The crystal used is the Reeves-Hoffman, type 13N3, 38.4 KHz ±.01%, crystal as specified in the purchase description.

2.4.2 NS2 Card - Shift Driver, Delayed Power Switches and RC Circuit

Printed circuit card NS2, shown in figure B-2 of Appendix B, contains the shift driver, power switches and shift voltage source. The shift driver is a monostable circuit which provides the two inputs required for the operation of the gated core-diode magnetic shift registers. The shift output provides the high current pulse for the magnetic core readout. The transfer output is a voltage pulse that allows the magnetic register capacitors to remain charged for the duration of the shift pulse; it returns to ground after the shift current pulse has ceased. This enables the magnetic register outputs (as well as the logic output for the first bit) to be stored into the appropriate bits of the magnetic register. The power switches provide power to logic gates, voters, and the register input circuits only during the transfer pulse. The shift voltage source is a simple R-C network to provide the source of the shift current. It is designed to minimize power supply loading, to gradually reduce the amplitude of the shift current pulse, and to provide a low current source for the reset and clear inputs.

The shift driver is activated by grounding an input to charge a small input capacitor through a high impedance path. The shift driver is triggered when the input ground is removed and the capacitor discharges through a low impedance path which includes a zener diode to set the trigger threshold. This triggering circuit provides protection against false

triggering. Once the input circuit has triggered, the in-phase output signal is fed back through a timing network to maintain the shift driver in the ON state for the desired period of time. The shift output is a current limited transistor stage which saturates if less than the maximum current at a positive voltage is available from the shift source. The transfer output is driven by a complementary (PNP-NPN) inverter stage in which neither transistor is conducting during the quiescent period. During the period that the shift driver is ON, the transfer output is driven by a low impedance to a voltage approximately 1 to 2 volts less than twice the supply voltage (approximately 10V). This double voltage is supplied by a capacitor which cannot discharge to a level below the supply voltage. Some "droop" on the transfer pulse is permissible because the highest voltage is necessary only during the magnetic read-out in the early portion of the shift pulse. The transfer output is driven to a low impedance to ground when the shift driver switches OFF, but the low impedance to ground is maintained only for a short period of time. A shunt resistor to ground provides a relatively high impedance path to ground for leakage currents during the quiescent period.

The delayed power switches are driven from one (or all three) of the transfer outputs from corresponding shift drivers. The delayed power switch output is simply a low impedance to the voltage supply during the transfer pulse, with a slow rise time to control decoder "spiking". Delayed power switching is used on all logic gates and voters in the magnetic logic to reduce the power requirements. The switched power clamped voltage output is used for the magnetic register input circuits to provide a relatively constant charging voltage for the input capacitor.

As described above, the shift voltage source is a simple R-C network. Energy for the shift current is stored in the capacitor; the resistor limits the current drawn from the power supply to that used for clear and reset. Because the shift driver is ON for a longer time than required for read of the magnetic bits, the capacitor value is chosen so that it becomes discharged during the shift pulse.

As indicated above, power switching is used for the majority voters. Each voter power switch has a diode OR gate input from all replicas of the same transfer pulse so that no failures propagate through voters. The voter power switch has a longer time constant to provide longer turn-on delay and insure elimination of spiking. It does not have a fast turn-off because it is not necessary and cannot be implemented in the simple manner used for the logic power switch without causing failure propagation through voters.

2.4.3 NS3 Card-Magnetic Registers

Printed circuit card NS3, shown in figure B-3 of Appendix B, contains five individual gated core-diode magnetic shift registers. These registers are the non-volatile storage elements of the sequencer system and are vendor supplied pre-packaged units. Each core of the magnetic register provides one bit of shift register storage. An input circuit is included for each register so that a logic signal may be used to set the first bit of the register. The input circuit, therefore, provides the semiconductor logic-magnetic register interface.

The operation of gated core-diode shift registers may be summarized as follows: Each core is wound with at least 3 different windings - a high current shift winding and two low current windings, one each for read-in and read-out. In addition, the first core is sometimes provided with an alternate shift winding which is wound in the opposite sense to permit setting the first core while clearing all remaining cores. Every core also has diodes in series with the read-out and read-in windings, and an output capacitor. Information is shifted through the register by the two-step operation of read-out, then read-in. The shift current provides the read-out operation by providing a sufficiently high reset current to induce a corresponding current in the read-out winding of any core not previously reset. This current flows through the read-out diode and charges the output capacitor. No current flows in the input winding if the transfer voltage is sufficiently high to reverse bias the read-in diode. There is, however, an induced voltage in the read-in winding, approximately equal to the voltage on the output capacitor of the same core. The output capacitor remains charged until the transfer line is grounded; this causes any of the charged capacitors to discharge through the read-in windirg and set the corresponding core. Any current flow through the read-out winding at this time is prevented by the read-out diode.

The magnetic register input circuit simply provides an additional output capacitor which may be discharged through the input winding of the first bit. In addition, there is a capacitor-charging resistor and a pullup resistor connected to the switched power voltage clamp from the shift driver. The capacitor is charged if a logical "0" (ground) is present on the input during the transfer pulse. A diode is included to insure a low impedance discharge path.

2.4.4 NS4 Card Buffers

Printed circuit card NS4, shown in figure B-4 of Appendix B, contains the buffers for the magnetic register-semiconductor interface. The buffers provide a high impedance load to the magnetic register outputs. Input to the buffers is through a diode OR gate. A logical "1" can be guaranteed on the buffer output by grounding the OR gate output through one or more diodes provided for that purpose.

The basic buffer circuit consists of 3 stages - a positive logic OR gate driving an emitter follower which drives an inverter output stage. Any positive input will cause the output to be a logical "0". However, if one of the inhibit inputs is grounded, this causes all inputs to be a logical "0" and therefore forces the output to be a logical "1". In addition, a high impedance discharge path is provided from the OR gate output which is connected to the transfer output of the shift driver. This path allows removal of charge from the OR gate integrating capacitor as well as from any magnetic register output capacitor not discharged by the transfer voltage (the last bit of every complete register has no other discharge path) and also provides a path for any leakage current.

2.4.5 NS5 Card-Power Failure Detector and Count Inhibit Circuit, Set Driver

Printed circuit card NS5, shown in figure B-5 of Appendix B, contains the power failure detector, count inhibit circuit and a set driver. The power failure detector inhibits the possible passage of count pulses down the divider chain when power supply conditions are such that improper logic operation might result. The power failure detector operates as a functional part of the divide-by-20 Counter by immediately inhibiting the one pulse per second output of this counter after either the loss of AC power or the restoration of DC power to the logic. The set driver circuit is used to insert the initial state in the divide-by-60 key stream generator register. It is activated by the restored output decoder and forces the register to contain the initial state (regardless of the previous state) after the end of the shift current pulse. Although there is no regeneration, the normal power supply input is buffered to help insure that power supply transients cannot cause spurious outputs. Two independent circuits are used to provide the inhibit output: one is specifically designed for loss of primary power; the other provides the turn-on inhibit. The diode input for the count inhibit is located on the power failure inhibit card as a matter of convenience.

2.4.6 NS6 Card-Relay Driver and Diode Array

Printed circuit card NS6, shown in figure B-6 of Appendix B, contains a relay driver, relay, and a diode array. A negative-going signal on any driver diode input causes the circuit to turn ON and remain ON for a fixed period of time. The set coil of the magnetically latching relay is energized during this time. A direct input which causes the circuit to be ON continuously and manual controls for setting and resetting the relay are also provided.

The relay driver circuit is essentially a monostable PNP-NPN two stage inverter with capacitor coupling to the first stage from either the output or the diode inputs. A special direct-coupled input is provided which is used for the Launch Clamp. Grounding this input causes the circuit to remain ON and completely discharge the output capacitor, thereby

preventing any further setting of the relay until the clamp has been released and the output capacitor allowed to charge. Grounding any input diode causes the circuit to turn ON and the output capacitor to discharge through the set coil of the relay. The feedback is coupled to the input through another diode, so that the input may be released at any time during the output pulse without affecting the output. Even if a diode input remains grounded, the circuit returns to the OFF condition. This permits manual setting of the relay, even though another diode input will not trigger the circuit.

A single timing network is used for both the input feedback and the input triggering. The coupling capacitor is normally discharged, with both sides referenced to the 6V. supply (which is connected to the emitter of the first stage), so that power supply transients (including power turn-on) do not trigger the circuit. A small integrating capacitor (also referenced to the 6V. supply) improves the input noise immunity and the rejection of possible spurious inputs.

2.4.7 NS7 Card-Digital Difference Detector

Printed circuit card NS7, shown in figure B-7 of Appendix B, contains the digital difference detectors used for the testing of the sequencer breadboard. There are two detector circuits on each card. These circuits are part of the test equipment and do not contribute to the functional operation of the sequencer. The difference detector card also contains connections for the forcing signals so that these controls are mechanically disconnected from any of the associated signals if the difference detector card is removed. The entire set of difference detectors permits complete checking of the logic redundancy of the sequencer. The difference detectors themselves are not triplicated; only one detector is associated with each voter input and voter output.

Two sets of diode gate inputs detect both the highest and lowest voltage input. If the highest exceeds the lowest by the threshold of the circuit, the detector transistor is turned on. If the lowest input under these conditions is also near ground (logical "0"), then the difference detector output becomes a logical "1". If the display control input is a "1", then any difference that persists for approximately 1.8 μsec will activate a logical feedback connection which will maintain the output at a logical "1". The minimum time required to latch the output is primarily determined by the integrating capacitor on the node of the feedback gate.

2.4.8 Standard Cards

The "Standard" printed circuit cards, as shown in figures B-8, B-9, B-10, B-11 and B-12 of Appendix B, are general card types containing commonly-used logic functions.

These cards include the following:

Figure	Type	Nomenclature of Card in Logic Diagrams
B-8	NAND Gate	002 or 002A
B-9	Parallel Register	004
B-10	Fan-in Gate	014
B-11	Positive Logic Driver	469
B-12	Resistor Board	030

The NAND Gate and Fan-in Gate cards offer convenient arrangements of diode-transistor integrated gate circuits. These include 3-input NAND gates with and without nodes, 8-input NAND gates and diode clusters. A modification of the NAND Gate card 002 to allow two separate power switched power inputs is explained in figure B-8 of Appendix B. The modification is designated 002A. The Parallel Register card contains twelve flip-flop circuits, groups of which share common clock inputs. The integrated circuits are MIL-tested versions of the Westinghouse and Raytheon 200 series line in TO-5 can packages.

The Positive Logic Driver card contains four positive logic drivers. These consist essentially of a 3 input AND gate capable of driving 100 ma bilateral current. Signal returns are provided for each signal output. The circuit is capable of withstanding temporary short circuits to ground at the output when all inputs are logical "1". The positive logic driver is used in the sequencer as a line driver to ground support equipment (for the Update Verify and the Clear and Counting signals) as well as a driver for test signals.

The Resistor Board is a universal card allowing the installation of various conventional components. It is used to mount pull-up resistors, isolation diodes, etc. when required and not available on other cards.

2.4.9 Redundant Power Distribution

The sequencer power distribution system is shown in figure A-10 of Appendix A. The primary power, as received by the sequencer breadboard, is DC power from the test chassis distributed on redundant lines. The +28V. power, for the relays, is received on 3 lines into a diode buffered node. The voltage at the node will be the highest of the three applied voltages. Note that the node connection can be disconnected so that different voltages can be applied, via the test chassis, to each replica. The power is fed from the node (via decoupling networks consisting of a fuse, diode, capacitor and bleeder resistor) independently to each replica of the system. The +6V. power distribution is similar to the +28V. power distribution except that the +6V. power is regulated power. The redundant power regulator

shown in figure B-13 of Appendix B accepts +12V. power from the test chassis and provides +6V. power to the sequencer system. The regulator is designed so that no single component failure can cause the output voltage to fail high. The regulator circuit provides very good regulation over the required temperature, loading, and input variations, as well as with single failures.

A bleeder resistor in the decoupling network maintains a minimum drain of 90 ma thru the output diodes to prevent loss of regulation in the diodes due to the low current requirements of the magnetic logic. The +6V. power requirements for each replica are broken into two parts. Each part is fed via a separate decoupling network from the +6V. node. The power sense signal, which indicates the imminent failure of +28V. and +6V. power, is derived from a special DC supply in the test chassis. It is fed from the power sense node to the power failure detectors in the Divide-by-20 Counter circuitry.

The vendor-supplied 12V and 28V power supplies located in the test chassis are shown schematically in figure B-14 and B-15 of Appendix B.

3. Test Program

3.1 Operational Tests

The normal starting condition of the sequencer, in the spacecraft, requires that the lower frequency counters must start in the "clear" state. To clear these counters, the COUNT INHIBIT is applied at the divide-by-20 counter and then the CLEAR is applied to the divide-by-60 and all succeeding counters. The COUNT INHIBIT signal stops the counting action of the lower frequency counters.

As indicated, each of the three replicas may be inhibited independently unless the INHIBIT DISABLE switch is on. This switch will release all of the COUNT INHIBIT lines, and allow simultaneous initial operation of the counters.

Since the normal starting condition of all of the lower frequency counters is the clear state with all relays reset, the CLEAR is switched on prior to the COUNT INHIBIT release. The CLEAR should extinguish the 1 MINUTE, 7 HOUR, and UPDATE VERIFY indicators and cause the CLEAR AND COUNTING indicator to light. The output relays are reset by the MANUAL RESET switches. The difference detector indicators may then be switched temporarily to LATCH OFF to extinguish any indicator set due to previously existing differences.

The RELAY INHIBIT, which is normally derived from the LAUNCH CLAMP, is simulated by the CLEAR AND COUNTING signal in the breadboard. Therefore, if the relay power is on, all relays will set when the CLEAR AND COUNTING SIGNAL is reset (light on) by the CLEAR. Therefore, all relays will normally require a MANUAL RESET following the CLEAR operation.

The X20 and X60 SPEED UP control switches should be OFF to provide outputs at the normal frequency. Either or both of the SPEED UP control switches may be ON to provide speed up factors of 20, 60, or 1200 times normal.

After the Sequencer Breadboard has been cleared and before the INHIBIT is released, the update operation as was described in Section 2.2 may take place. The 7 HOUR output toggle flip-flop indicators are used to monitor the update operation. The UPDATE ENABLE switch must be ON; otherwise, the update pulses will be counted as normal 1 MINUTE inputs and the entire Launch Counter will be affected. An update switch is provided for each replica in the breadboard. However, to obtain proper operation of the system, a simultaneous update must be applied to all three replicas. Simultaneous update signals can be obtained by connecting the three replicas together at the update inverter gate outputs (test point 1 or pin 3 at card location 02). The first pulse generated by the update push button should generate a 7 HOUR

output and therefore change the state of the output indicator from OFF to ON. The divide by 7 ring in the Launch Counter then advances one position for each update pulse; this should generate a 7 HOUR output for every 7 input pulses and cause the output indicator to change state. The final position of the divide by 7 ring is determined by the number of input pulses in excess of exact multiples of 7. Each update pulse should also result in an UPDATE VERIFY output which will cause the UPDATE VERIFY indicator to change state. If the Sequencer has been cleared before the update operation, the update input pulses should have no other effect than to cause the 7 HOUR outputs and provide the UPDATE VERIFY output.

The COUNT INHIBIT may be released from each replica individually by turning OFF separate COUNT INHIBIT switches or from all replicas simultaneously by turning ON the INHIBIT DISABLE switch. If each replica is released individually, the starting time is the time at which the second COUNT INHIBIT switch is switched OFF. Individual switching of the COUNT INHIBIT switches is normally expected to cause differences on the 1 SECOND output due to lack of initial synchronism.

Sequencer operation after the release of COUNT INHIBIT should be as follows:

The 1 MINUTE output indicators will immediately (within one-twentieth of a second) change from OFF to ON. The 7 HOUR output indicator will change state once for every 7 X 60 = 420 minutes, with the timing of the first output dependent upon the initial state of the divide by 7 ring as determined by the update operation. The L-1 relay will be set after 56 minutes and set pulses will occur again every 68 minutes. Likewise, the L-2 relay will be set after 60 minutes and set pulses will occur every 60 minutes thereafter. The L-3 relay will be set after 60 X 17 = 1020 minutes and set pulses will occur every 1020 thereafter. However, the setting of L-3 will set both L-1 and L-2 (if not already set) and inhibit any further set pulses to them.

The purpose of the voter difference detectors is to monitor the voter outputs to verify that all voters in the same "file", or location, always provide the same logical output. Proper operation of the voter difference detectors (and voter forcing switches) is verified by applying all possible combinations of inputs to the voter difference detectors (using the voter forcing switches) and observing that there is a voter difference indication whenever the inputs are not all alike. Dynamic operation of the difference detectors is checked by forcing each single replica to a 1 and observing that the difference detectors latch ON at the time of the first output pulse from the associated processor or voter.

There are several procedures that may be used to provide all 8 combinations of the 3 inputs to the voter difference detectors, for the static difference detector tests. Perhaps the simplest procedure for manipulating the switches is as follows:

1.) With the VOTER LATCH switched off, switch all voter forcing switches to the "0" state. All voter indicators should remain OFF. Individually switch each forcing switch to the "1" state and return to the "0" state. Observe that all voter indicators should remain ON while each of the switches is switched to "1" and should go OFF after returning each switch to the "0" state.

2.) Switch all voter forcing switches to the "1" state. All voter indicators should remain OFF. Repeat the procedure described above, moving each switch from "1" to "0" and returning to "1".

The voter difference detector tests are intended to verify that the voter difference detectors and their forcing switches are operating. However, the probability is high that even if a voter difference detector does not indicate a failure in normal operation, that failure will still be detected by processor difference detectors. Therefore, it is not expected that these tests would be conducted frequently. It should also be noted that the system is rendered inoperative by the complete test procedure described above. If it is desired to leave the system operative as much as possible, only one forcing switch should be applied at a time. The system can then be operated dynamically on the remaining lines. If operation is attempted while using the voter forcing switches, the processor difference detectors will also indicate differences.

The purpose of the processor difference detectors is to provide a continuous monitor of the processor outputs to majority voters. The operation of both the processor forcing switches and the processor difference detectors is verified by the singular rank testing procedure as outlined below, or in exactly the same manner as the voter forcing switches and voter difference detectors as outlined above.

The processor difference detectors normally indicate all logic errors generated at the processor outputs to majority voters. However, singular rank testing is necessary to verify that each non-redundant replica can actually operate independently, with the other replicas disabled, and that the voters are capable of transmitting correct signals under these conditions. If the voter difference detectors are monitored during singular rank testing, it can be verified that the voters all provide the same majority output for all possible inputs. Singular rank testing is intended for use in an operating system, with proper system operation throughout the tests.

The singular rank testing procedure is summarized as follows:

1.) The system is operated in all normal functional modes. If the difference detectors indicate that there are logic errors present, they should be repaired; otherwise the system will fail during the singular rank tests.

2.) One rank is chosen as the normally operating non-redundant system. Its processor forcing switch must be left in the normal non-forcing mode. One of the remaining forcing switches is switched to the "0" state, the other to the "1" state. The processor difference detectors are observed to verify that the use of any two forcing switches in opposite states causes the indicators to be ON. (If the system is operating with outputs of both "1's" and "0's" to voters, the use of any one forcing switch should cause a difference indication). If all of the detectors indicate processor differences for all the combinations of forcing inputs, then it is verified that all processor detectors and forcing switches are operative.

3.) The system is operated to verify that the rank chosen for normal operation is capable of correct operation for the desired conditions. If it is desired to further check for the possibility of unknown coupling between ranks (other than at the voters), the states of the two remaining forcing switches may be reversed and the operational test repeated.

4.) The procedure described above is essentially repeated for the remaining replicas. The replica formerly forced to the "0" state is now switched to the normal mode, the other forcing switch is reversed from the "1" state to the "0" state, and the switch previously in the normal mode is switched to the "1" state. Operation of the detectors and system functional capability is verified as before.

5.) The procedure is repeated again, with the last replica (previously forced to the "0" state) now switched to normal mode, the other forcing switch reversed, and the switch previously in the normal mode switched to the "1" state. Operation is verified as before.

The proper operation of elements throughout the system verifies that all processors are operating correctly and that the voters are capable of transmitting correct signals. In addition, if there is no voter difference indication during the procedure described above, then the voters provide the majority output for all possible inputs.

The difference detectors may be operated in two modes, either continuous indication or display latch. When the indicator latch switch is ON, any output from the difference detector will cause the indicator to latch and remain ON; when the indicator latch switch is OFF, the indicator provides a continuous display of the difference detector output. Separate indicator control switches are provided for the voter and processor detectors. The voter detectors should be operated with the indicator latch ON except during the voter detector testing procedure. The processor detectors should be operated with the indicator latch OFF during the singular rank testing procedure. The processor indicator latch should be ON during normal operation.

The ability of the unit to tolerate power failures without loss of existing counter states is tested by turning off the AC power, at the test chassis, for measured time intervals and noting that the system outputs still function with the proper timing after the measured time interval. Note that the time interval measurement must take into account the built in time delay of the power failure detector (approximately 3.0 sec.) in addition to the time the AC power is off.

The equipment was tested, as described above, over the temperature range from -10° C to +85°C with the three DC power inputs (from the test chassis) varied, in all combinations, over a ±15% voltage range. In addition, the susceptibility of the unit to single component failures was tested: 1.) by opening and shorting components in the oscillator and power distribution circuitry and 2.) by removal of cards and single rank forcing in the circuit redundant circuitry.

3.2 Test Results and System Changes

This section includes a description of the problems that were encountered during the test program and the design changes that were made to the system in order to obtain the desired system operation. Minor changes, such as wiring list corrections and the addition of pull-ups will not be discussed.

The only design change in the clock divider chain, including the Divide-by-4, Divide-by-480, Divide-by-20, and Divide-by-60 counters, was the addition of the clock to the output decoding in the Divide-by-480 counter. This input provides the same functional input as the switched power input, which is a necessary input in the all 0's decode in order to provide an output with AC transitions to trigger the following shift driver. The clock input to the 480 count decode was included as a matter of convenience to provide comparable timing for either decoder.

There were a few changes in the 7-bit register in the Launch Counter. These changes were required by the timing problems which occur when a switched power voter is used directly on the output of a buffer, rather than on the output of a decoding gate. This problem occurs because the output of a switched power voter cannot be a 0 until its power has been turned on. The power turn-on must be slow to prevent spiking on the voter output, so that there is a significant delay between the beginning of the shift driver XFER pulse and the application of full power to the voters. This delay presents no problem (and is actually desirable) when voters are placed on the outputs of decode gates, which are 0 on the output only when the output signal or synchronizing feedback is present. In the case of a ring counter buffer, however, it is a 0 every clock pulse when the output or feedback signal must be inhibited. When the inhibit is delayed, however, a significant spike occurs on the output and feedback signals before the inhibit is applied. The only functional effect of this spike occurred on the feedback signal which was also wired to the buffer inhibit. This addition, compared to the former logic design, was made to limit the total possible number of 1's in a ring counter in case of a failure which might insert consecutive 1's in the register. However, if this inhibit is applied during any of the states of the counter which should contain a 1 in a magnetic bit, it rapidly destroys that information, even though the inhibit is applied only momentarily. Therefore, significant spikes which existed on the buffer inhibit could not be tolerated. Disconnecting the buffer inhibit eliminated this problem and does not affect the functional operation in any way. Since all other functional signals contain a high degree of integration and a high level of noise immunity, the voter turn-on delay did not affect the functional operation of the sequencer. However, the sensitivity of the test equipment is such that incorrect operation was indicated on the test panel.

The 7 HR indicator would toggle from the spike on the 7 HR decoder which resulted from the timing delay on the voter. This was corrected by placing an integrating capacitor with a discharge resistor on the input of the decoding gate.

In addition, the normal voter placement on the output of a decoding gate results in the timing of voter turn-off being determined by the turn-off of gate power or the XFER signal from the shift driver. In the case of the voter on the buffer output, the voter remains on until either the buffer turns off, or the voter power is turned off. Since the last bit of a magnetic register normally has a very slow discharge time, the voter turn-off for this case was determined by the turn-off of the voter power. Normal variations in this timing would cause the difference detectors to indicate under certain conditions. This indication was eliminated by reducing the discharge time for the last bit by connecting the buffer inhibit to the XFER signal via an isolating diode and a lower resistor than otherwise provided for the discharge path.

The distribution of the voter and gate switched power has been changed to include two more voter switched power gates in addition to the 16 available on a single standard card. The two logic gates that were cha .ged to voter power are the voter gates formerly connected to gate power. The switched power to the 1PP7HR decode is necessary to inhibit the gate when there is no shift driver XFER pulse.

The common input power connection for both the B1 and B2 magnetic shift registers (formerly pin 36 at the magnetic register card, NS3) was disconnected and brought out to separate pins. This was necessary to prevent the inadvert charging path which otherwise results in feedback from the first bit of one to the first bit of the other when these bits are an internal part of a shift register, as used in the 17-bit register in the Launch Counter.

The shift driver was slightly modified to reduce the shift current rise time. This was necessary to reduce the 0 noise of the magnetic registers. It was determined that the reduction of noise immunity at high temperature, due to reduced diode thresholds, was sufficient to permit the register to regenerate zero noise to a logical 1. The shift current rise time was reduced by adding a capacitor from base to ground on the current-limiting driver transistor. In addition, the trimming shunt resistor on the emitter current feedback resistor was removed to slightly reduce the shift current.

The power distribution was changed slightly so that the power to the voters driving the Launch Counter shift driver is connected to the same section of power as the remainder of the Launch Counter. This was done because the voters are actually part of the Launch Counter, since the failure of such a voter causes the entire Launch Counter to fail in that replica. Actually, the combination of multiple functions on common cards does not permit the exact division of power distribution into the proper sections, since the Divide-by-60 counter shift driver, gate power switch, and voter power switch are all on one card. Therefore, the failure of Launch Counter power will also cause failure of the Divide-by-60 counter. Failure of the power distributed to the primary divider chain, however, will also cause failure of all clock outputs, including the 1PPMIN and 1PP7HR because the buffers in card locations 9 and 10 are shared among the Divide-by-20 counter, the Divide-by-60 counter, and the 7-bit register of the Launch Counter. If buffer card location 10 power were changed to Launch Counter power, then failure at the primary clock divider chain power would affect only the clock outputs through the Divide-by-60 counter.

In addition to the modifications and changes described above, there were several modifications of a minor nature which did not affect the functional operation. The more significant of these are listed below:

a. The test inputs from switches on the test panel for CLEAR and Voter 0 forcing were amplified through spare positive logic drivers in card location 22 to reduce the current required through the test cable and switches. Pullups are included on both of these inputs, of course, with capacitors added to the voter 0 forcing input to improve noise immunity.

b. Drivers were added to all of the toggle indicators (1PPMIN, UPDATE VERIFY, and 1PP7HR). It was found that the switched power voters and the switched power update verify gate, due to the slow power turn on (or the lack of pullups on the gate) did not provide the fast negative-going transition necessary to insure reliable triggering of the flip-flops. In the case of UPDATE VERIFY, the problem was solved simply by changing the existing driver; in the remaining cases a spare gate connected to DC power was inserted on the input.

c. Several minor modifications were made to the initial configuration to improve noise immunity and reduce noise sensitivity to the test panel switches. These included the addition of pullups to all forcing switch inputs, the use of a resistor-capacitor combination on switches to reduce the generated switch noise, and the use of coaxial cable on the update input to reduce noise pickup on that input as well as the addition of an inverter gate on the update pulse to the Launch Counter shift driver.

Appendix A - Logic Diagrams

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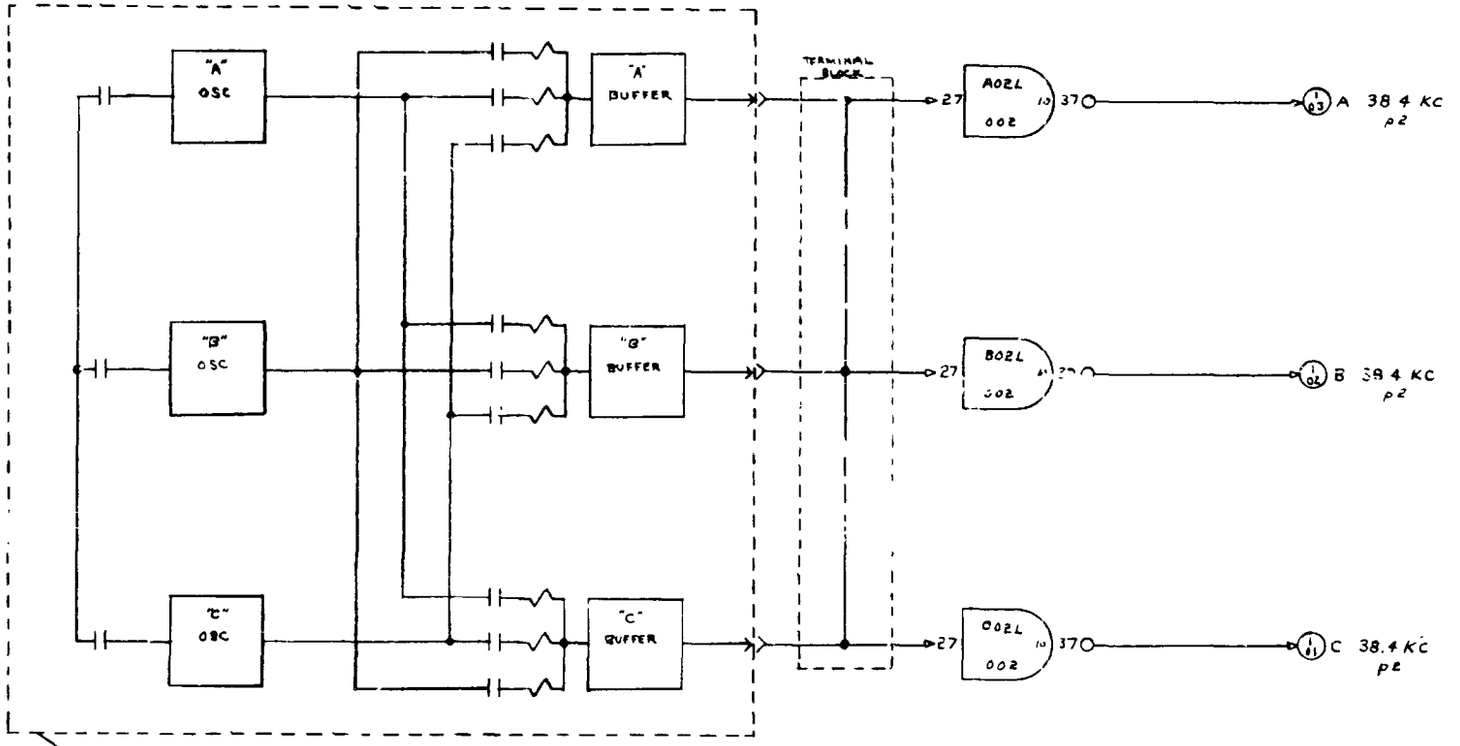
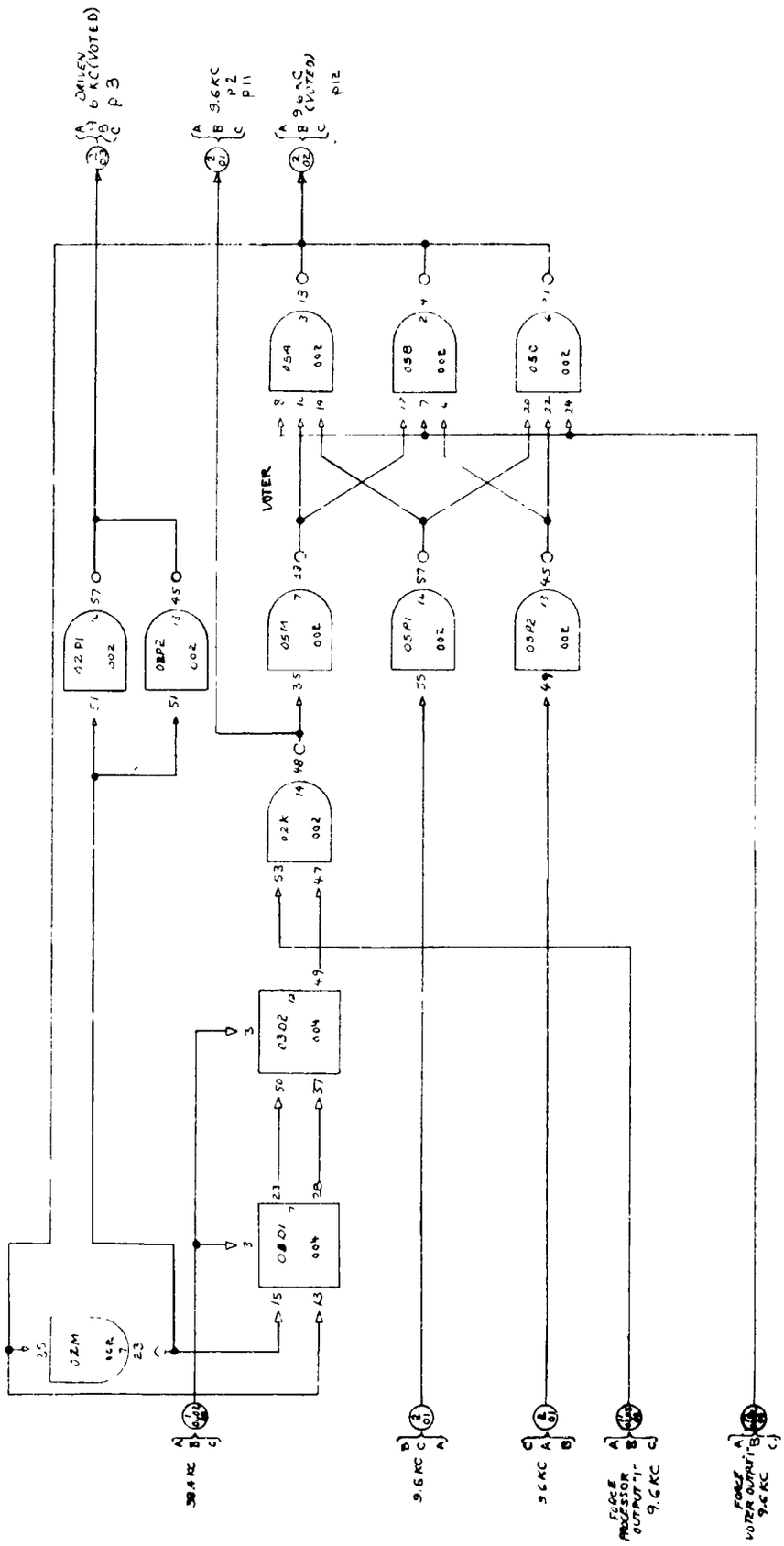


FIG A-1
38.4 KHz CLOCK
(REDUNDANT SKETCH)

A-1

WESTINGHOUSE ELECTRIC CORPORATION
AEROSPACE DIVISION
BALTIMORE, MD., U. S. A.



REVISIONS

ENGINEERING SKETCH

TITLE: FIG A-2 DIVIDE-BY-4 COUNTER

ENG.

APPROVED

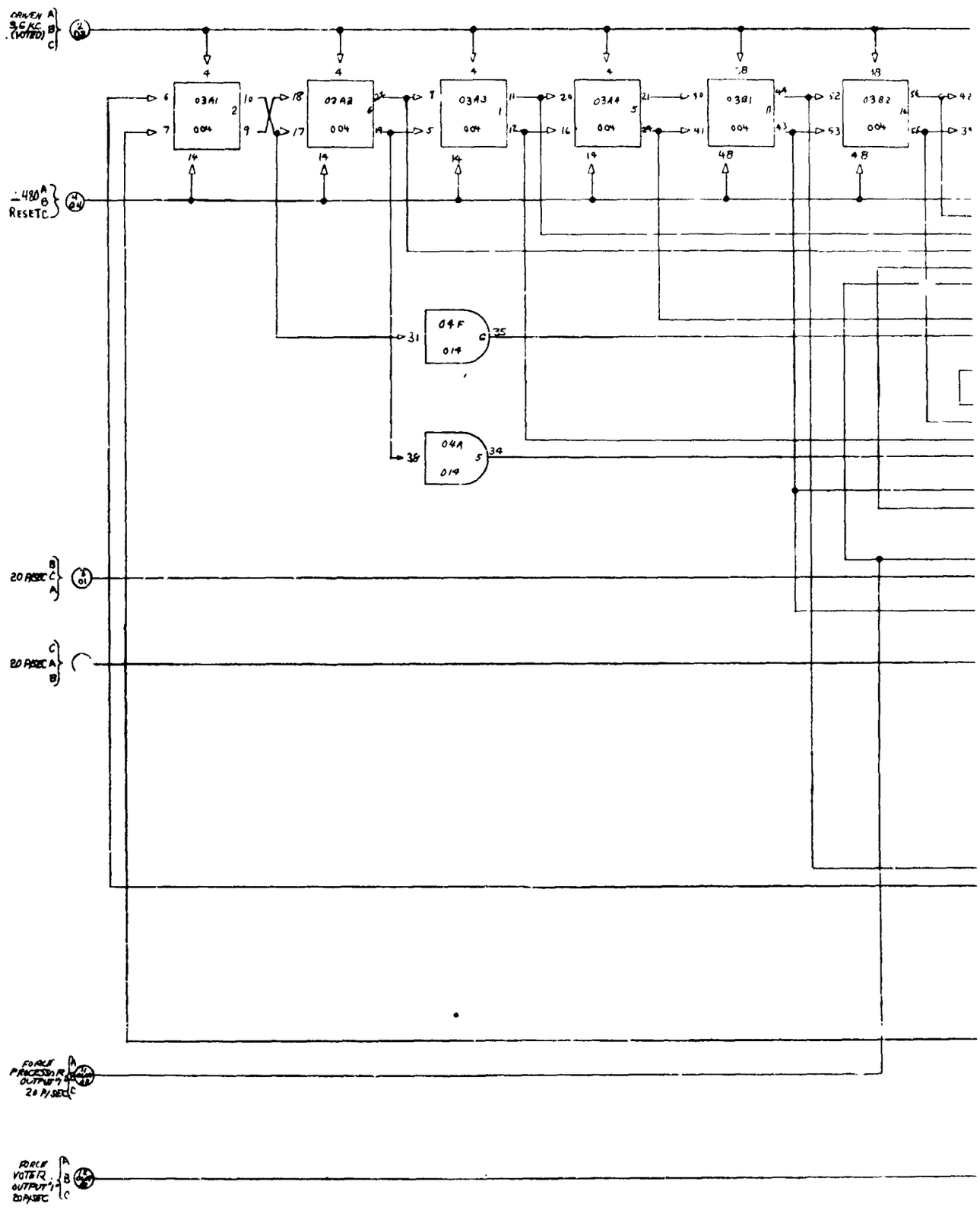
CHARGE

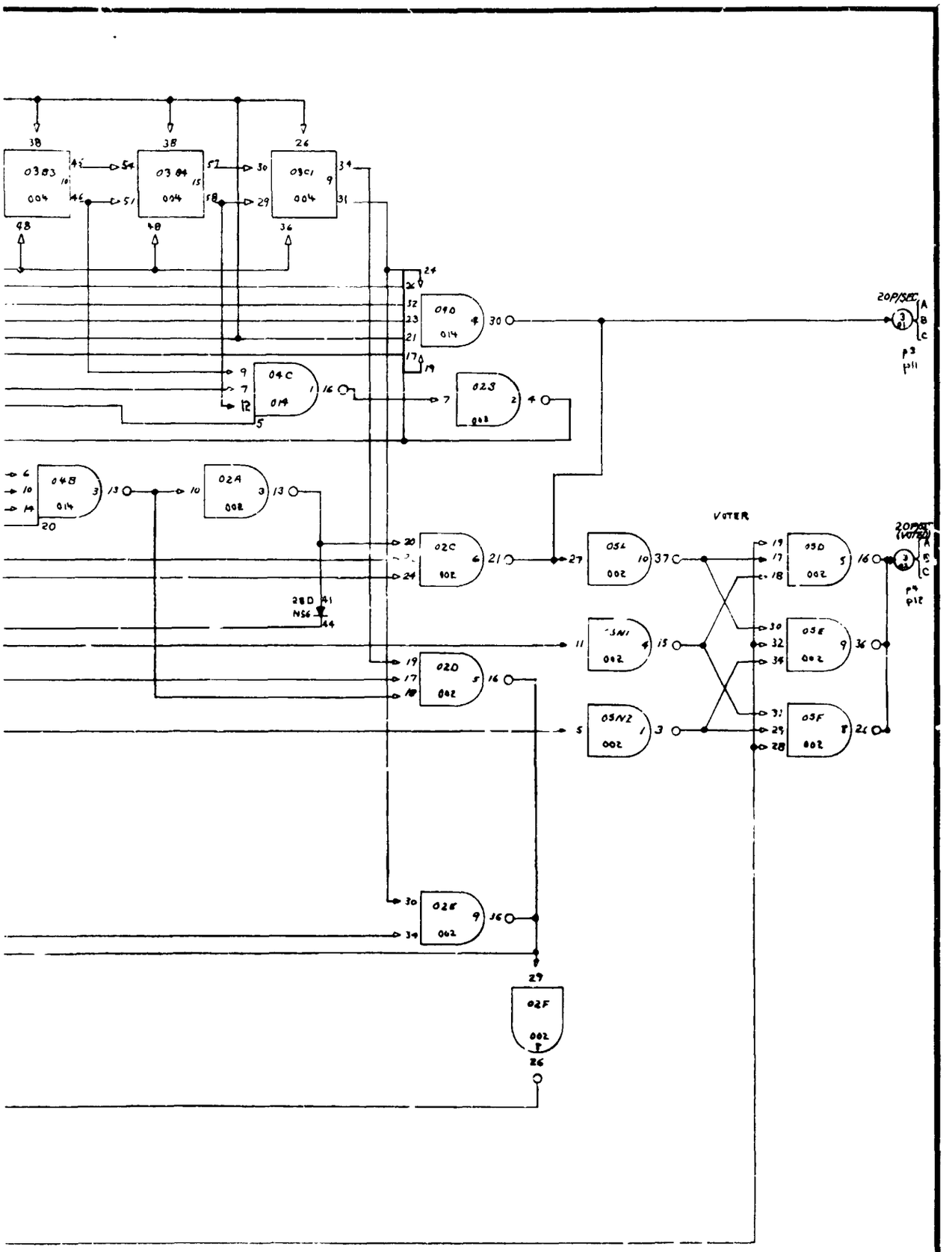
A-2

WESTINGHOUSE ELECTRIC CORPORATION
SURFACE DIVISION
BALTIMORE, MD., U. S. A.

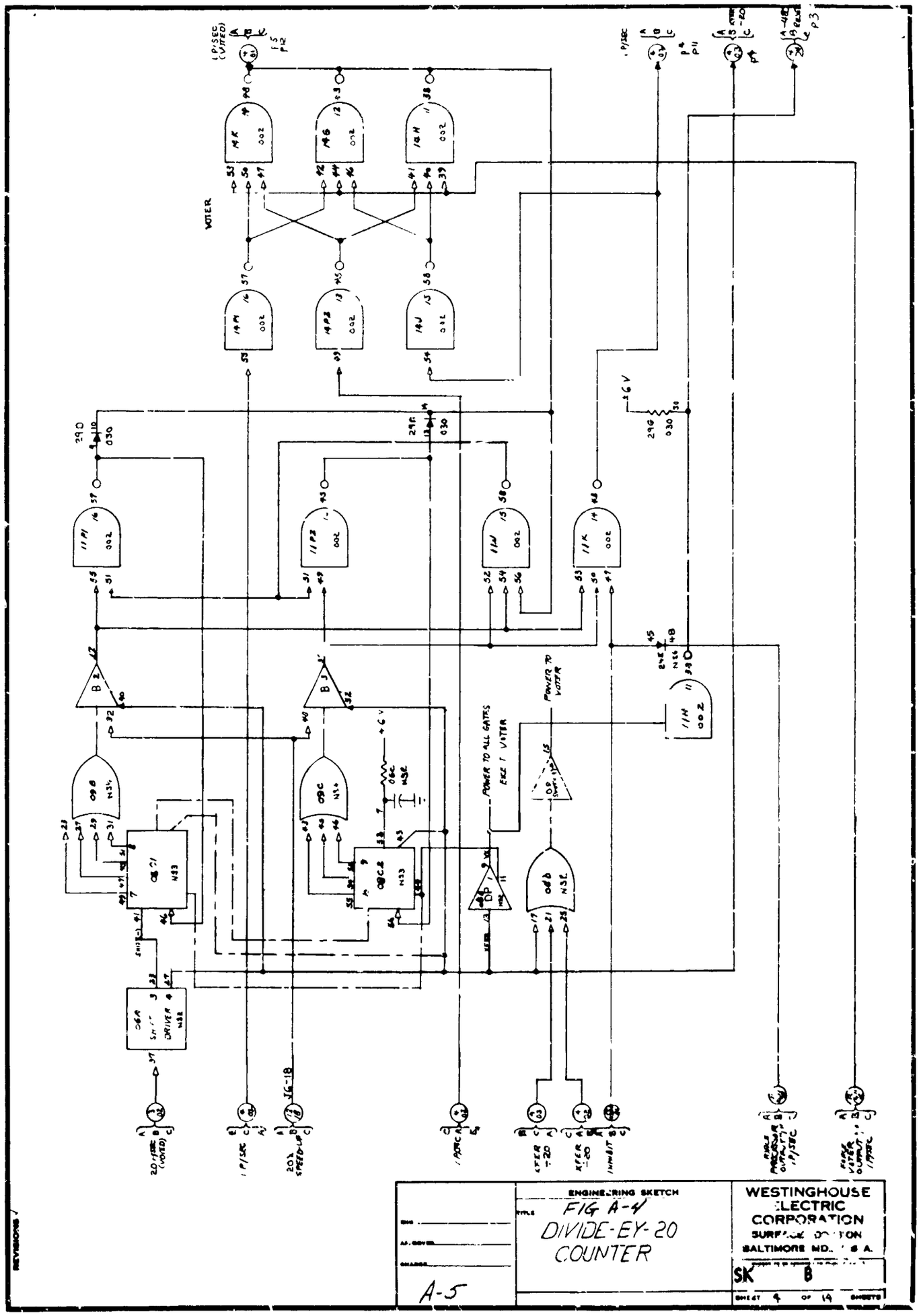
SK B

SHEET 2 OF 14 SHEETS


DRIVEN SYNC (NOTE 20)
-480 RESET
20 PPSEC
20 PPSEC
FORCE PROCESSOR OUTPUTS 20 PPSEC
FORCE VOTER OUTPUTS 20 PPSEC
0341
0042
0343
0344
0381
0382
004
04F
04A
014



ENG.	ENGINEERING SIZE	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE FIG A-3 DIVIDE-BY-480 COUNTER	SURFACE DIVISION
CHANGE		BALTIMORE, MD., U. S. A.
A-3/4		SK C
		SHEET 3 OF 14 SHEETS



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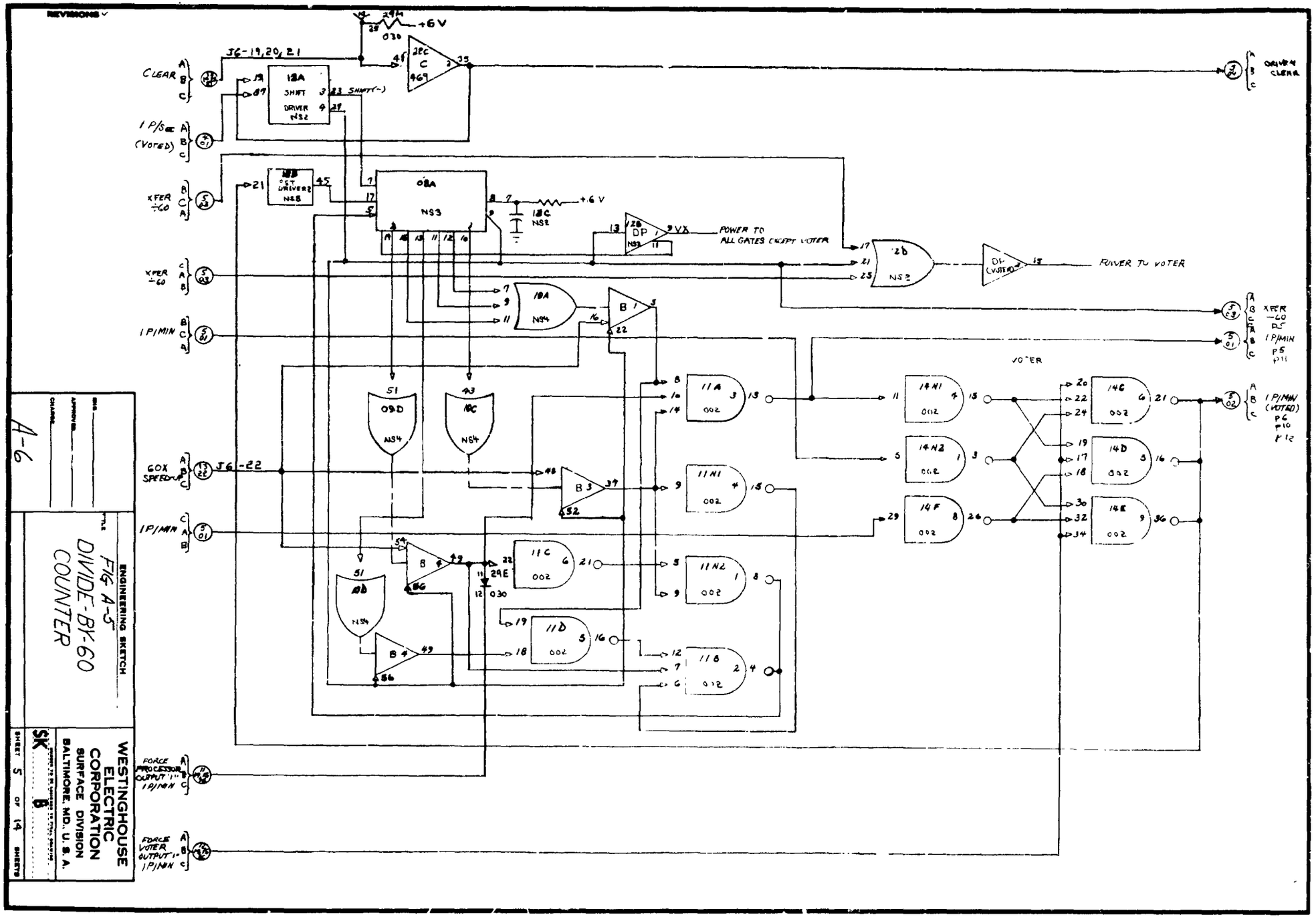
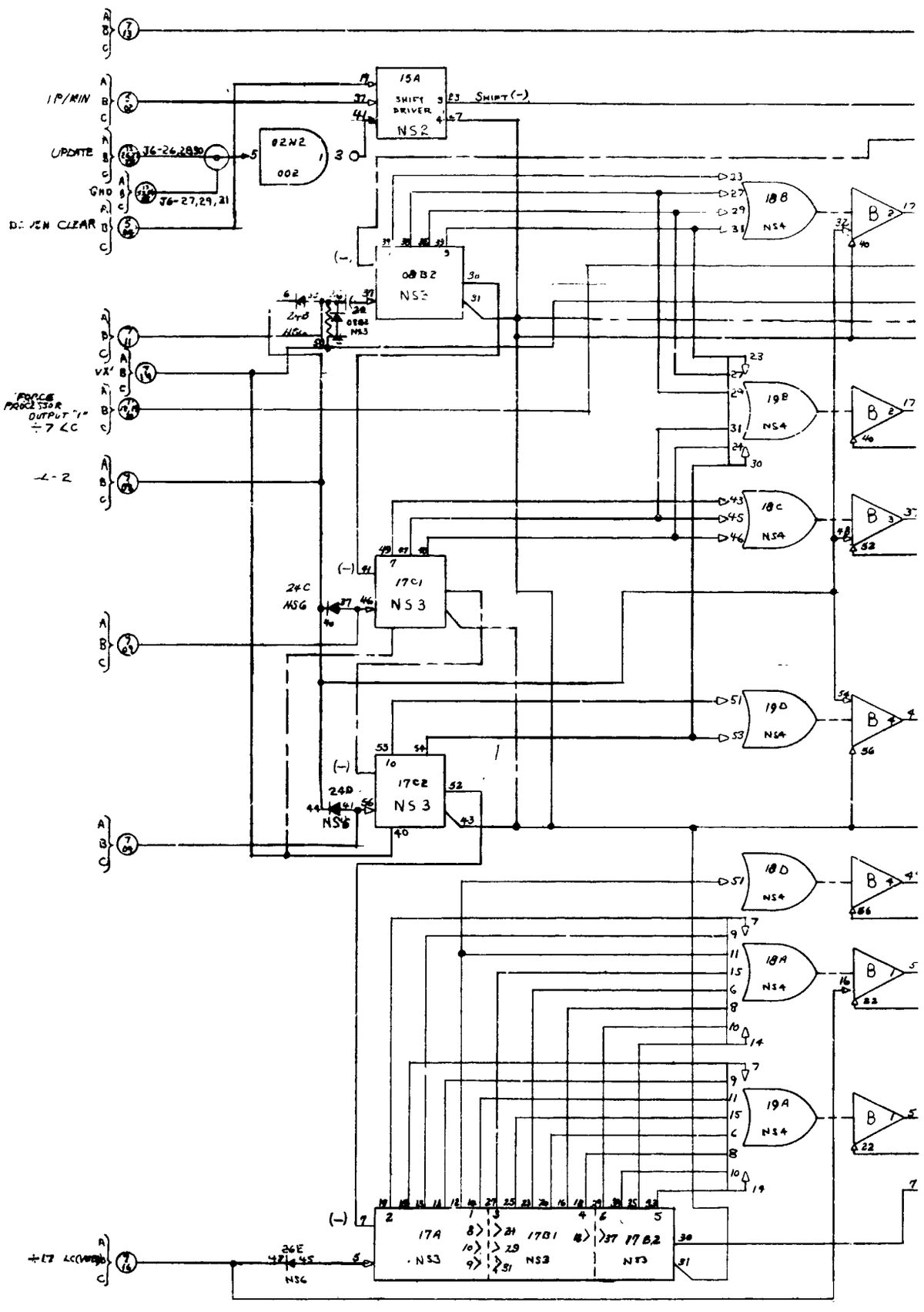

REVISIONS
+6V
CLEAR
I P/S (VOTED)
XFER -60
XFER -60
I P/MIN
GOX SPEED UP
I P/MIN
FORCE PROCESSOR OUTPUT "1" I P/MIN
FORCE VOTER OUTPUT "1" I P/MIN
POWER TO ALL GATES EXCEPT VOTER
POWER TO VOTER
VOTER
XFER -60 P5
I P/MIN P5 P11
I P/MIN (VOTED) P6 P10 P12
ENGINEERING SKETCH
FIG A-5
DIVIDE-BY-60 COUNTER
WESTINGHOUSE ELECTRIC CORPORATION
SURFACE DIVISION
BALTIMORE, MD., U. S. A.
SK
SHEET 5 OF 14 SHEETS
A-6


I/P/MIN
UPDATE
GND
DRIVEN CLEAR
FORCE PROCESSOR OUTPUT "1" ÷7 ∠C
∠-2
+17 ∠C
15A
SHIFT DRIVER
NS2
SHIFT(-)
02N2
002
J6-26,28,30
J6-27,29,31
08B2
NS2
17C1
NS3
17C2
NS3
17A
NS3
17B1
NS3
17B2
NS3
18B
NS4
18C
NS4
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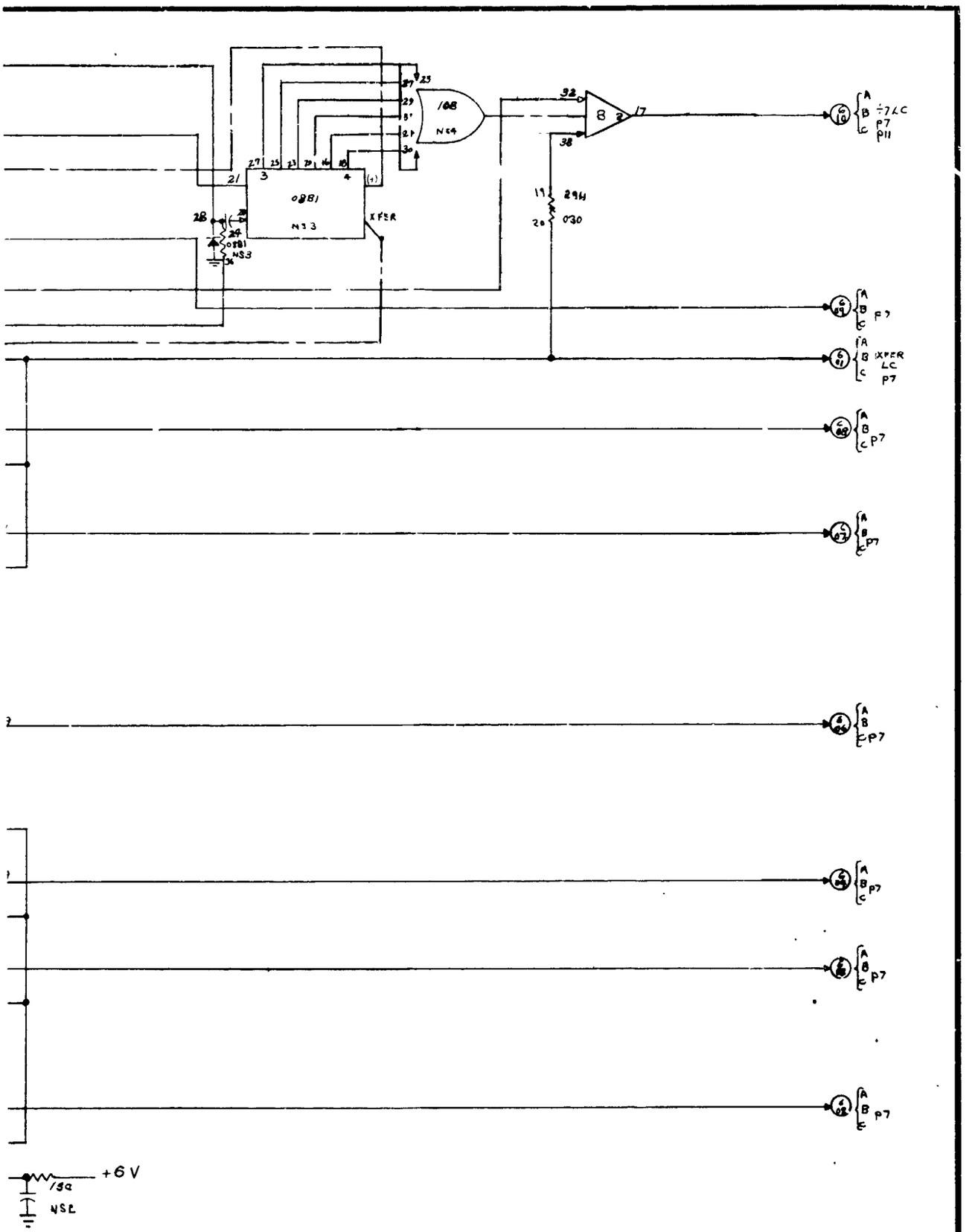
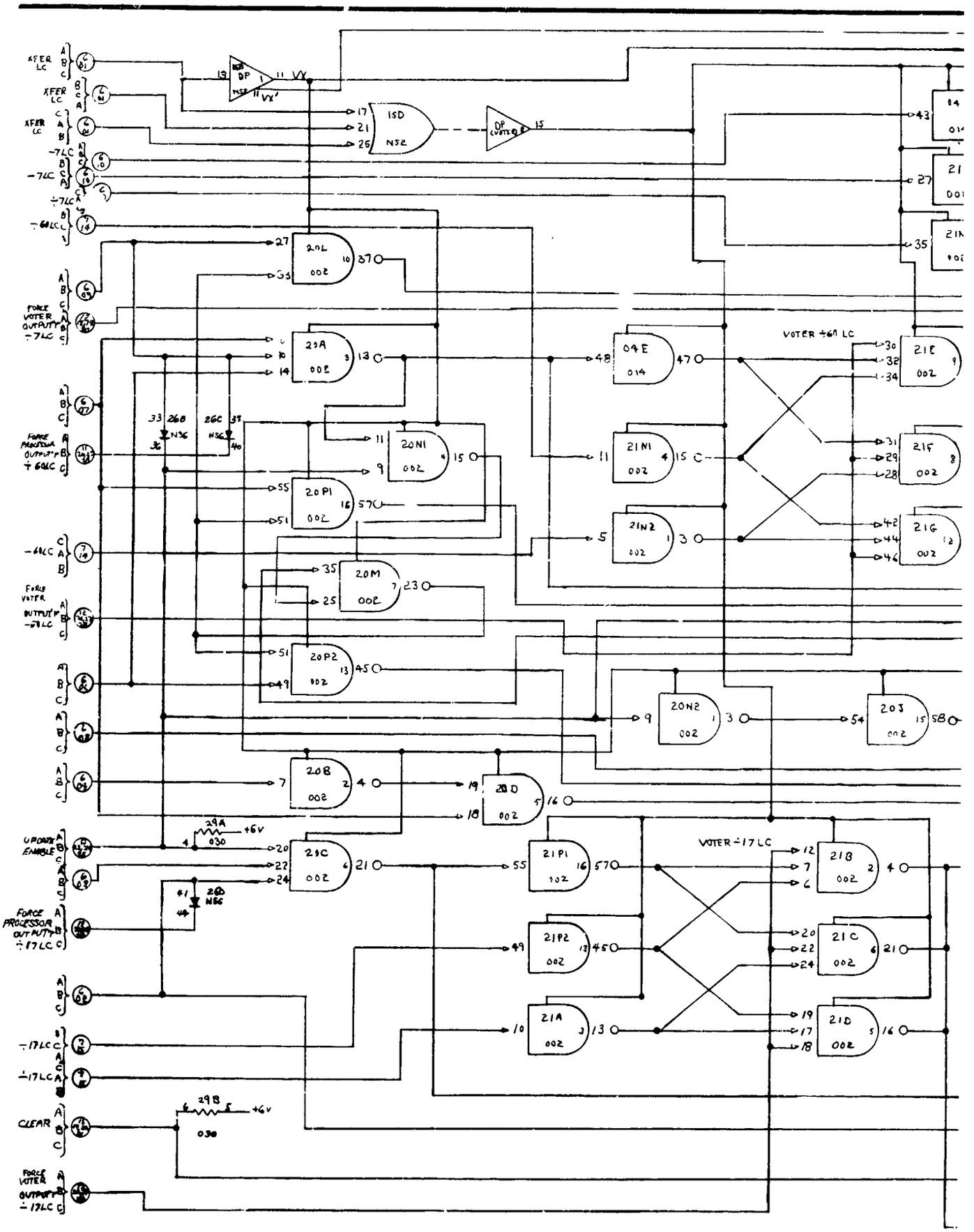
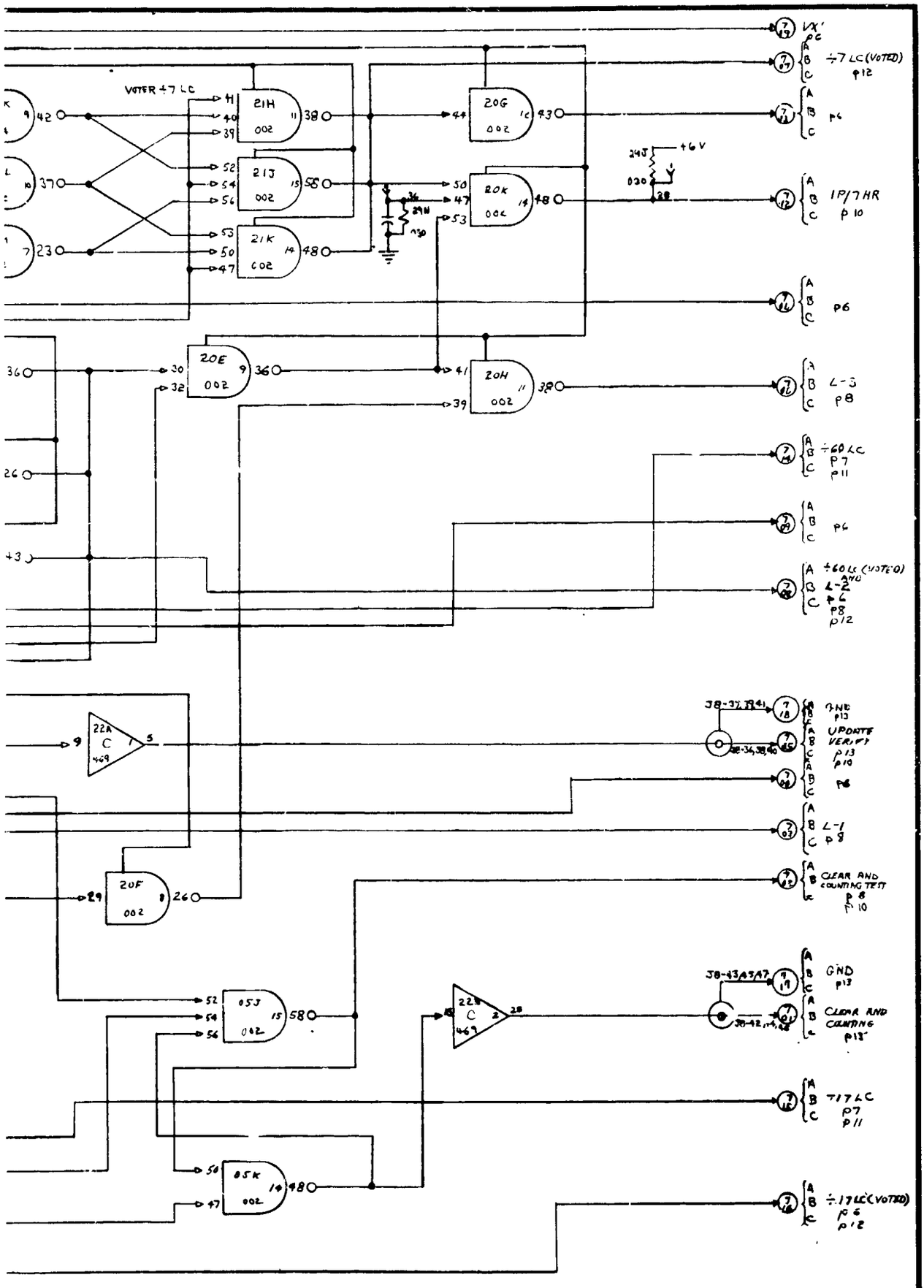
19A
NS4
24C
NS6
24D
NS6
26E
NS6

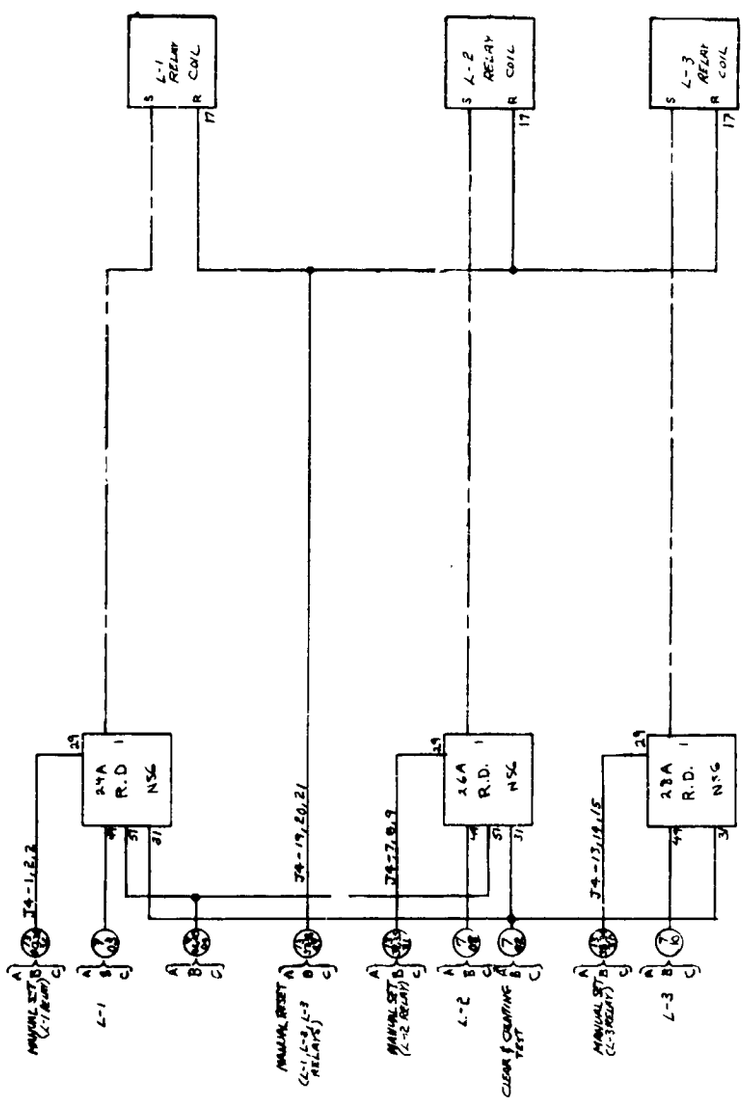


ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE FIG A-6 LAUNCH COUNTER REGISTERS AND BUFFERS (Sheet 1 of 2)	SURFACE DIVISION BALTIMORE, MD., U. S. A.
CHANGE		SK C
A-7/8		SHEET 6 OF 14 SHEETS

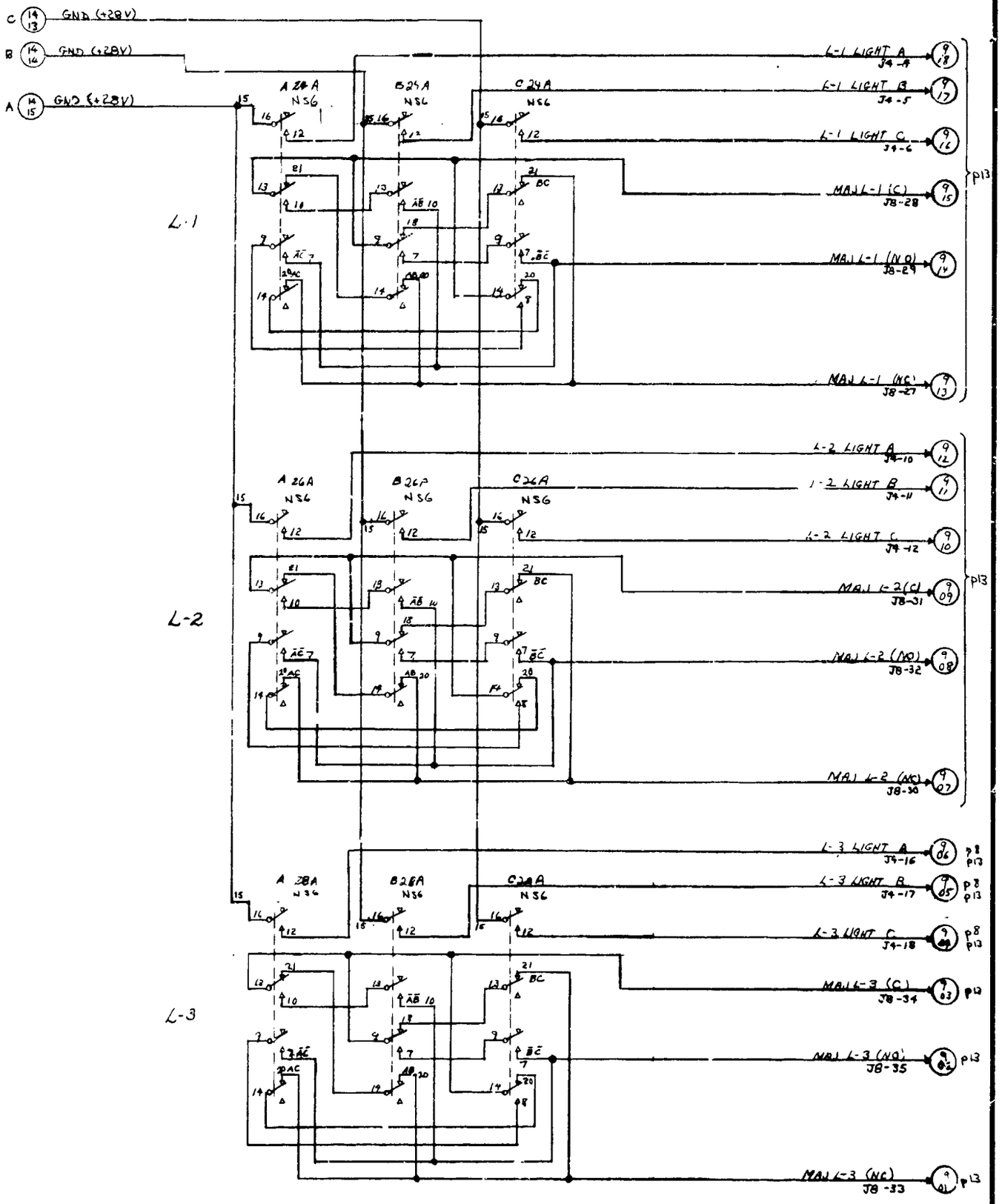

XFER LC
XFER LC
XFER LC
-7LC
-7LC
÷7LC
÷6LC
FORCE VOTER OUTPUT ÷7LC
FORCE PROCESSOR OUTPUT ÷6LC
-6LC
FORCE VOTER OUTPUT -6LC
UPDATE ENABLE
FORCE PROCESSOR OUTPUT ÷17LC
÷17LC
÷17LC
CLEAR
FORCE VOTER OUTPUT ÷17LC
DP
15D
20L
20A
20N1
20P1
20M
20P2
20N2
20B
20C
20D
04E
21N1
21N2
21P1
21P2
21A
VOTER ÷6A LC
21E
21F
21G
VOTER ÷17LC
21B
21C
21D
20J
29A +6V
29B +6V
NSG
REVISIONS



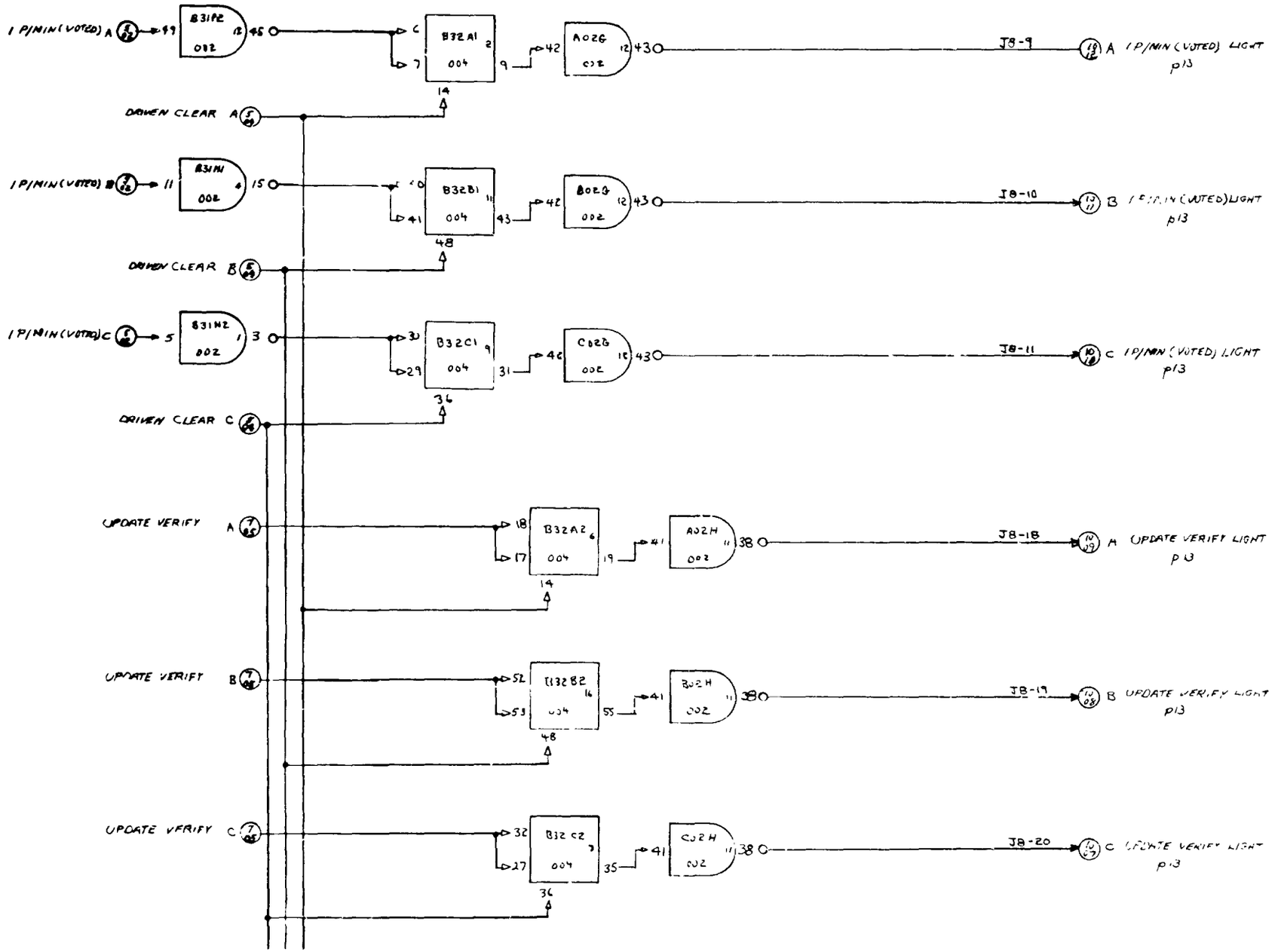
ENG. A-9/10	ENGINEERING SKETCH TITLE FIG A-6 LAUNCH COUNTER DECODE AND VOTERS (Sheet 2 of 2)	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK C SHEET 7 OF 14 SHEETS

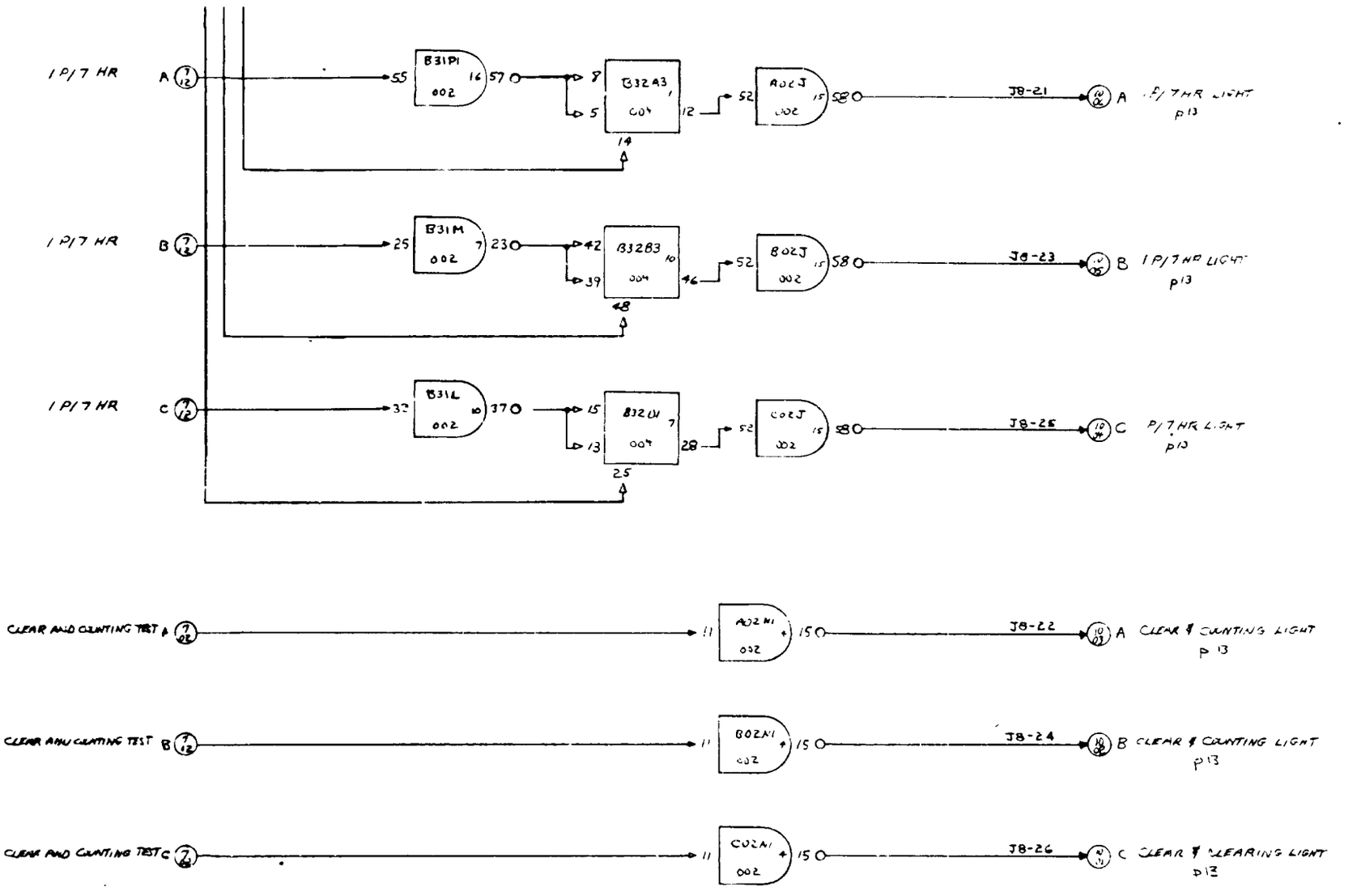


ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE FIG A-7 LAUNCH COUNTER RELAY CIRCUITRY	SURFACE DIVISION
CHARGE	RELAY COIL WIRING (Sheet 1 of 2)	BALTIMORE, MD., U. S. A.
A-11		SK B
REVISIONS		SHEET 8 OF 12 SHEETS



ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE: FIG A-7	ELECTRONICS DIVISION
CHARGE	LAUNCH COUNTER RELAY CIRCUITRY	BALTIMORE, MD., U. S. A.
A-12	RELAY CONTACT WIRING (Sheet 2 of 2)	SK B
REVISIONS		SHEET 9 OF 14 SHEETS


I P/MIN (VOTED) A
B31P2
002
DRIVEN CLEAR A
B32A1
004
A026
002
J8-9
A I P/MIN (VOTED) LIGHT
p13
I P/MIN (VOTED) B
B31N
002
DRIVEN CLEAR B
B32B1
004
B026
002
J8-10
B I P/MIN (VOTED) LIGHT
p13
I P/MIN (VOTED) C
B31N2
002
DRIVEN CLEAR C
B32C1
004
C026
002
J8-11
C I P/MIN (VOTED) LIGHT
p13
UPDATE VERIFY A
B32A2
004
A02H
002
J8-18
A UPDATE VERIFY LIGHT
p13
UPDATE VERIFY B
B32B2
004
B02H
002
J8-19
B UPDATE VERIFY LIGHT
p13
UPDATE VERIFY C
B32C2
004
C02H
002
J8-20
C UPDATE VERIFY LIGHT
p13



ENGINEERING SKETCH

TITLE: FIG. A-P TEST LOGIC

1P/MIN, UPDATE VERIFY, 1P/7 HR, CLEAR & COUNTING LIGHT INPUTS

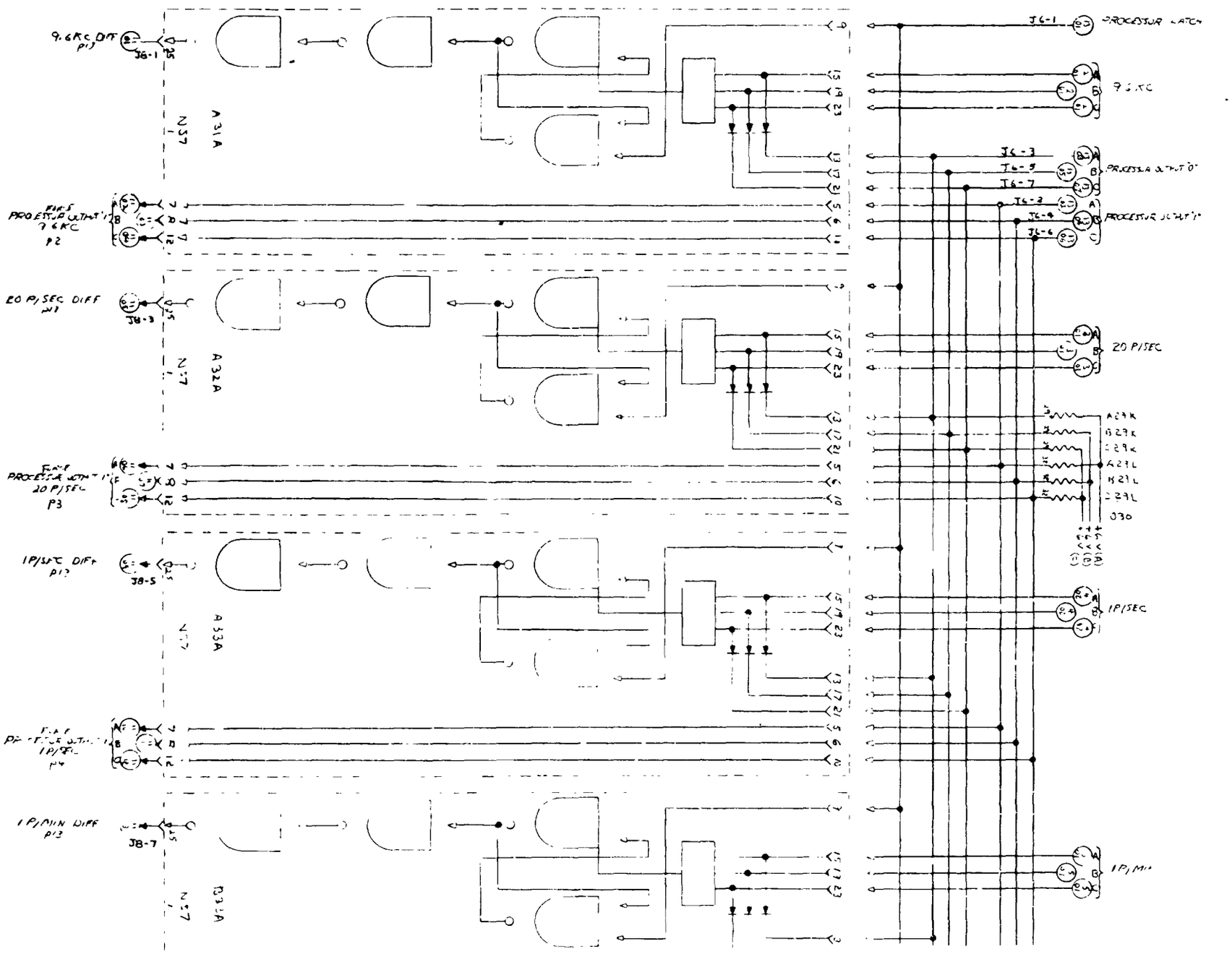
A-13/14

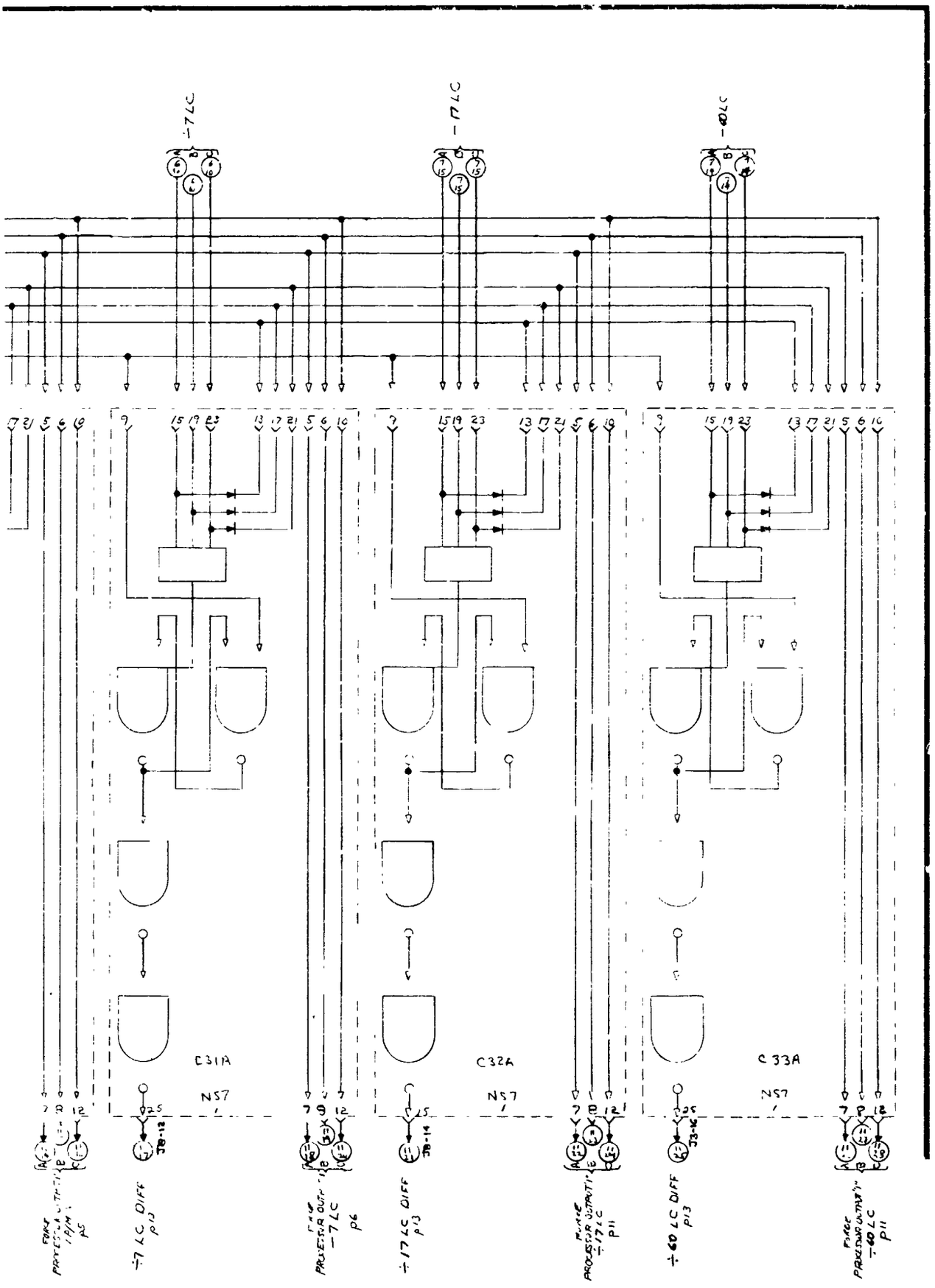
(Sheet 1 of 3)

WESTINGHOUSE ELECTRIC CORPORATION
SURFACE DIVISION
BALTIMORE, MD., U.S.A.

SK ..... C .....

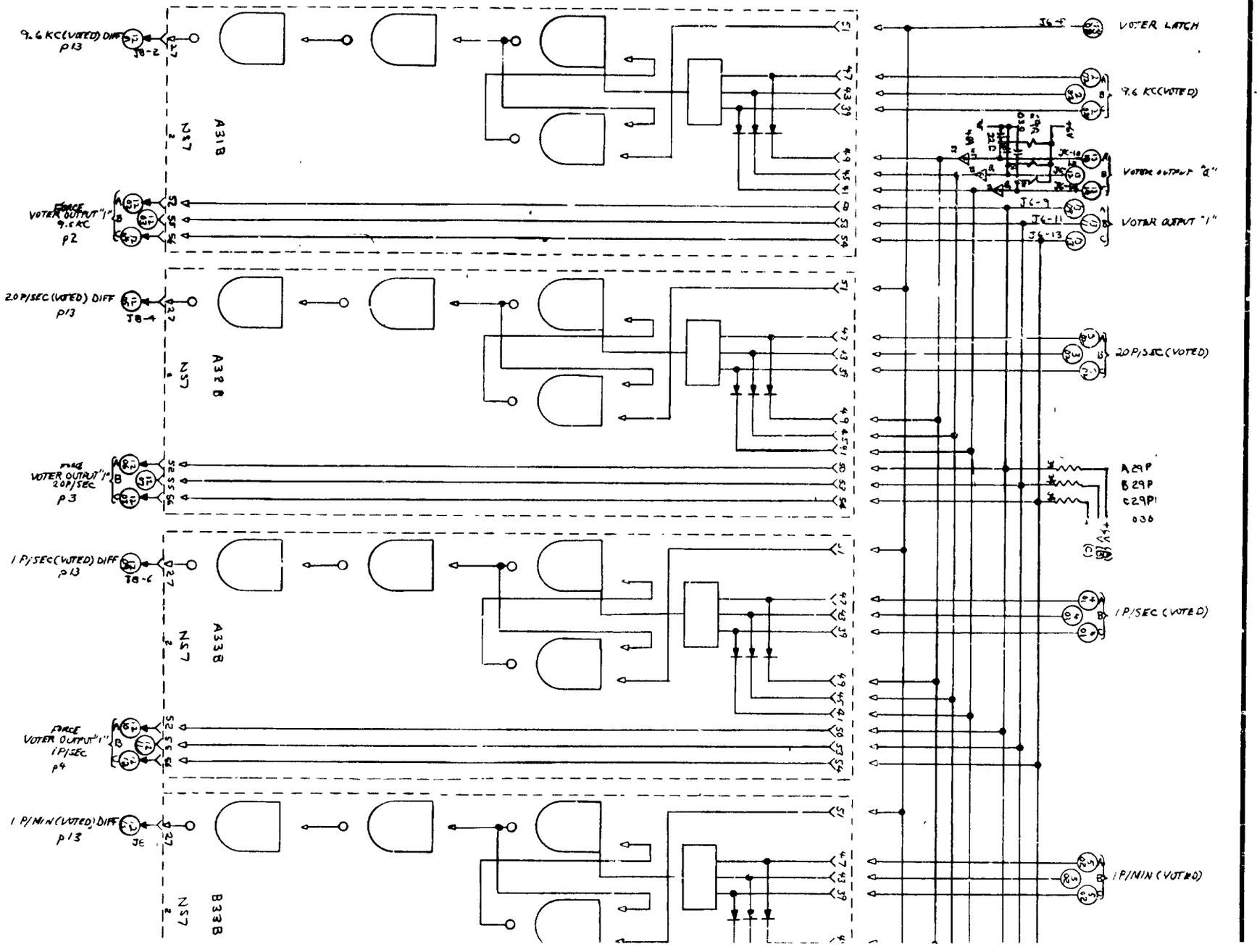
SHEET 10 OF 14 SHEETS

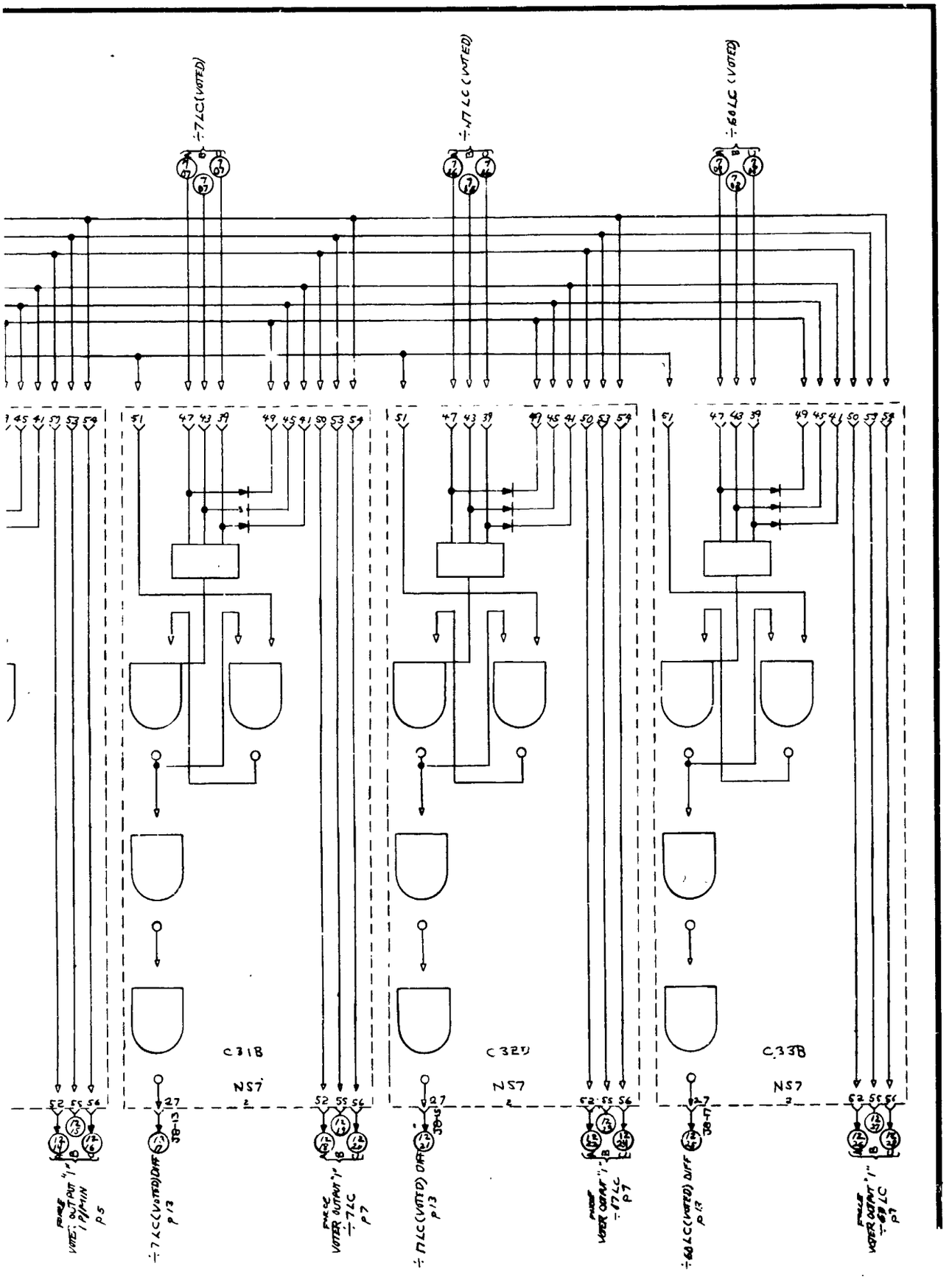

9.6KC DIFF
P1
J8-1
A31A
N37
PROCESSOR LATCH
J6-1
9.6KC
20 P/SEC DIFF
P1
J8-3
A32A
20 P/SEC
1P/SEC DIFF
P1
J8-5
A33A
1P/SEC
1P/MIN DIFF
P1
J8-7
A34A
1P/MIN
J6-3
J6-5
J6-7
J6-2
J6-4
J6-6
PROCESSOR OUTPUT "0"
PROCESSOR OUTPUT "1"
A29K
B29K
C29K
A29L
B29L
C29L
030



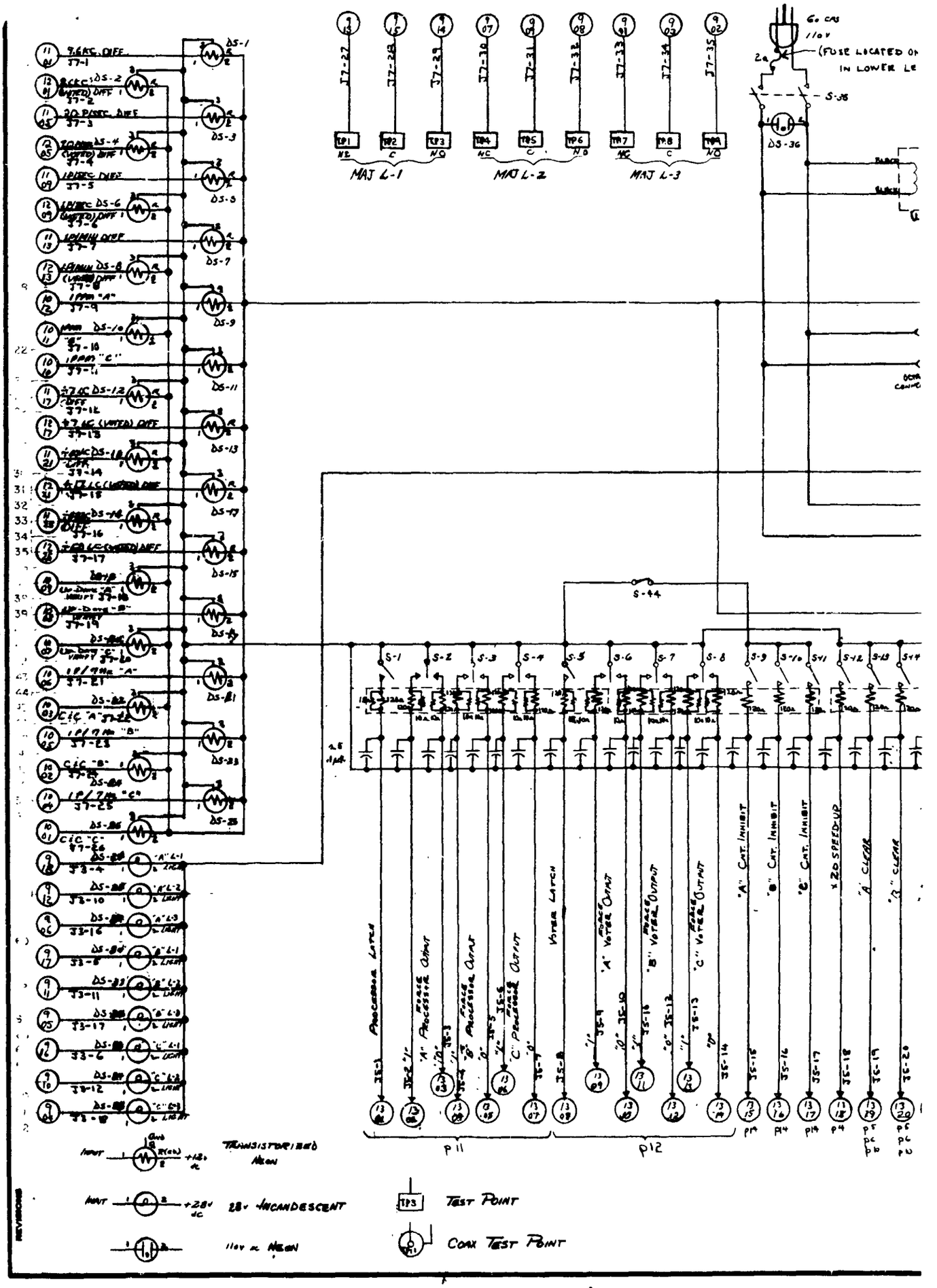
ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE FIG A-8 TEST LOGIC PROCESSOR DIFFERENCE DETECTORS (Sheet 2 of 3)	SURFACE DIVISION BALTIMORE, MD., U. S. A.
CHARGE A-15/16		SK C
		SHEET 11 OF 14 SHEETS

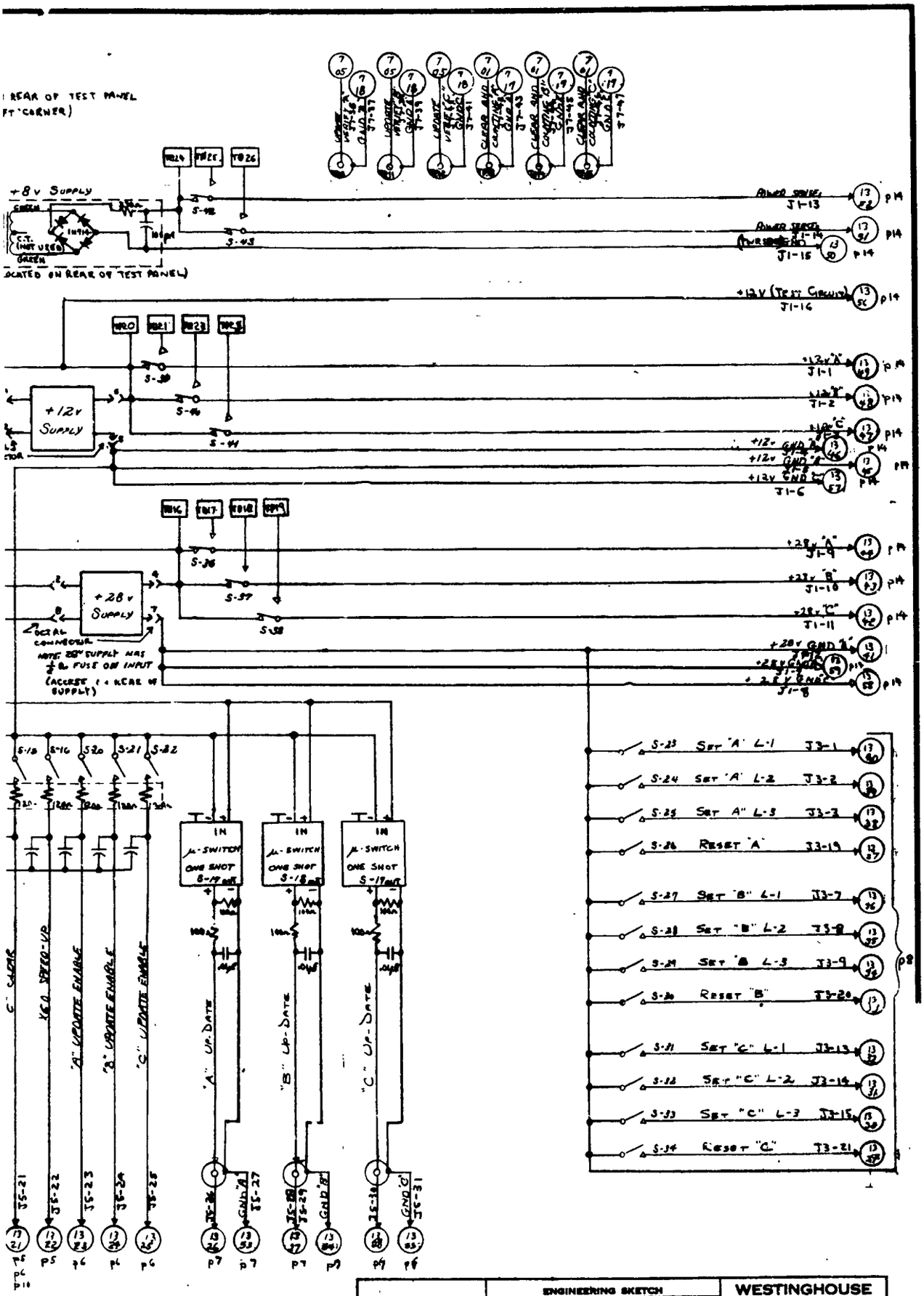
REVISIONS


9.6 KC(VOTED) DIFF
P13
J8-2
A31B
N57
FORCE VOTER OUTPUT "1" 9.6 KC
P2
20 P/SEC (VOTED) DIFF
P13
J8-4
A32B
FORCE VOTER OUTPUT "1" 20 P/SEC
P3
1 P/SEC (VOTED) DIFF
P13
J8-6
A33B
FORCE VOTER OUTPUT "1" 1 P/SEC
P4
1 P/MIN (VOTED) DIFF
P13
J8
B33B
VOTER LATCH
9.6 KC(VOTED)
VOTER OUTPUT "0"
VOTER OUTPUT "1"
20 P/SEC (VOTED)
A29P
B29P
C29P
030
1 P/SEC (VOTED)
1 P/MIN (VOTED)



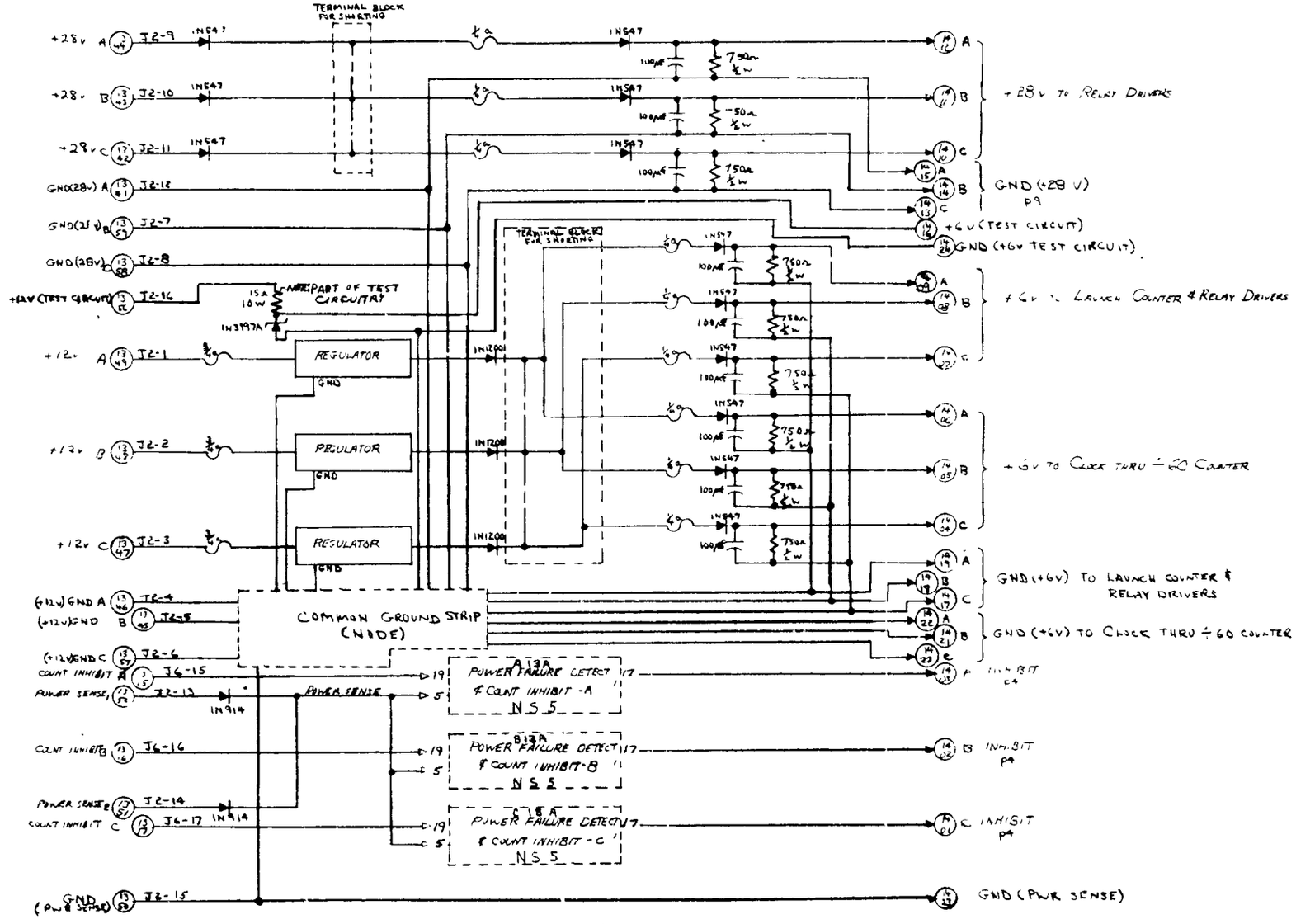
ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE FIG A-8	SURFACE DIVISION
CHARGE A-17/18	TEST LOGIC	BALTIMORE, MD., U. S. A.
	VOTER DIFFERENCE DETECTORS	SK C
	(Sheet 3 of 3)	SHEET 12 OF 14 SHEETS


J7-27
J7-28
J7-29
J7-30
J7-31
J7-32
J7-33
J7-34
J7-35
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
MAJ L-1
MAJ L-2
MAJ L-3
S-38
DS-36
S-44
P11
P12
TRANSISTOR/LED
NEON
28v INCANDESCENT
110v NEON
TEST POINT
COAX TEST POINT



	ENGINEERING SKETCH TITLE FIG A-9 TEST CHASSIS DIAGRAM	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD. U. S. A.
BY A. APPROVED CHANGE A-19/20		SK C SHEET 12 OF 14 SHEETS

REVISIONS



NOTE: TWO IN914 DIODES ABOVE (IN POWER SENSE CKT) ARE LOCATED ON LARGE VECTOR BOARD OF REAR PANEL.

NOTE: ABOVE CIRCUITRY LOCATED ON SMALL VECTOR BOARD ON REAR PANEL EXCEPT (1) REGULATOR POWER TRANSISTORS ARE ON REAR PANEL ITSELF (2) +6V (TEST CIRCUIT) ZENER DIODE IS ON REAR PANEL, 15A, 10W RESISTOR IS ON LARGE VECTOR BOARD OF REAR PANEL

A-21

ENGINEERING SKETCH

TITLE: FIG A-10 POWER DISTRIBUTION SEQUENCER CHASSIS (REDUNDANT SKETCH)

BID
APPROVED
CHANGE

WESTINGHOUSE ELECTRIC CORPORATION
SURFACE DIVISION
BALTIMORE, MD. U.S.A.

SHEET 14 OF 14 SHEETS

SK B

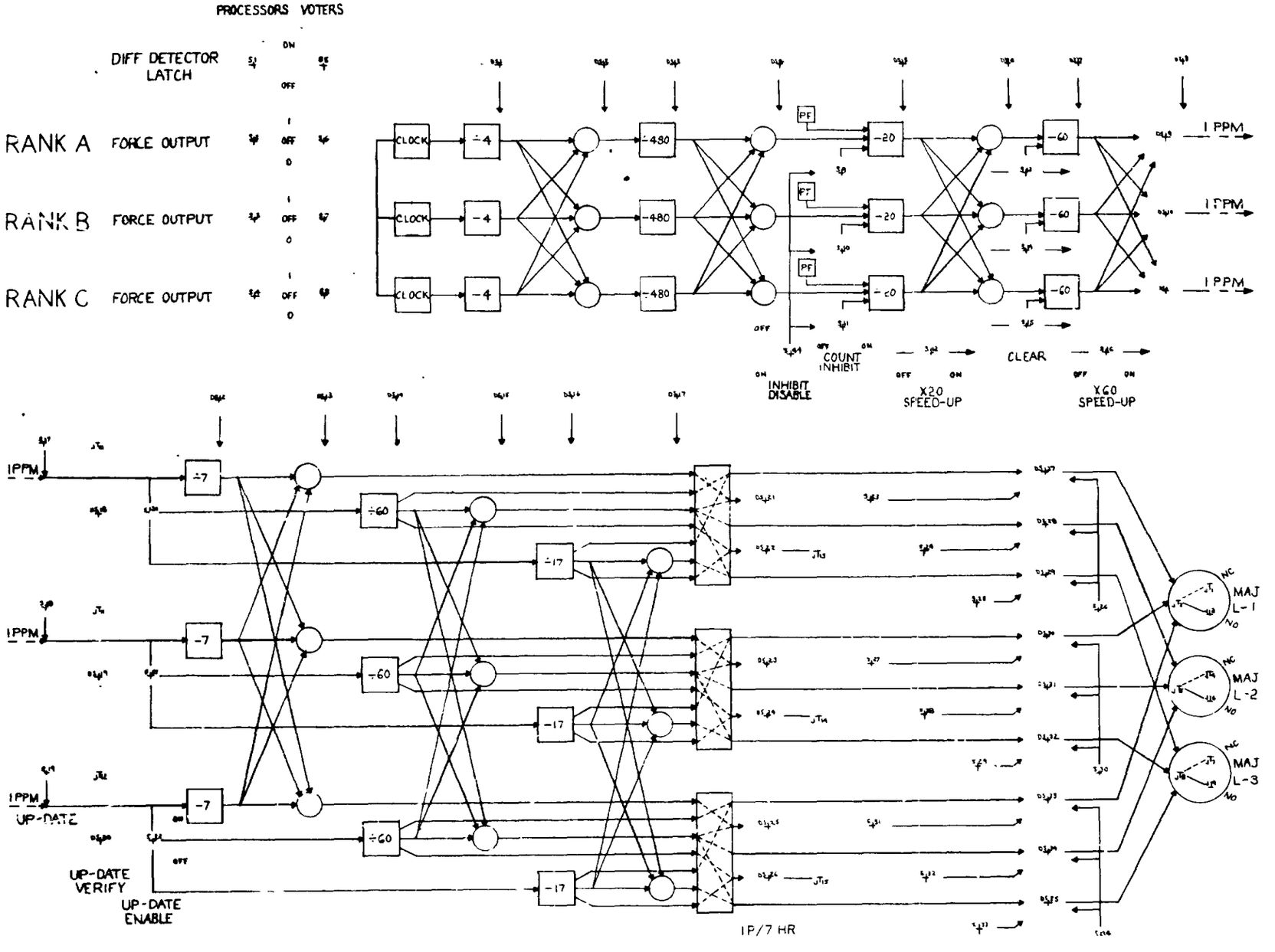
FIGURE A-11. CARD ASSIGNMENT

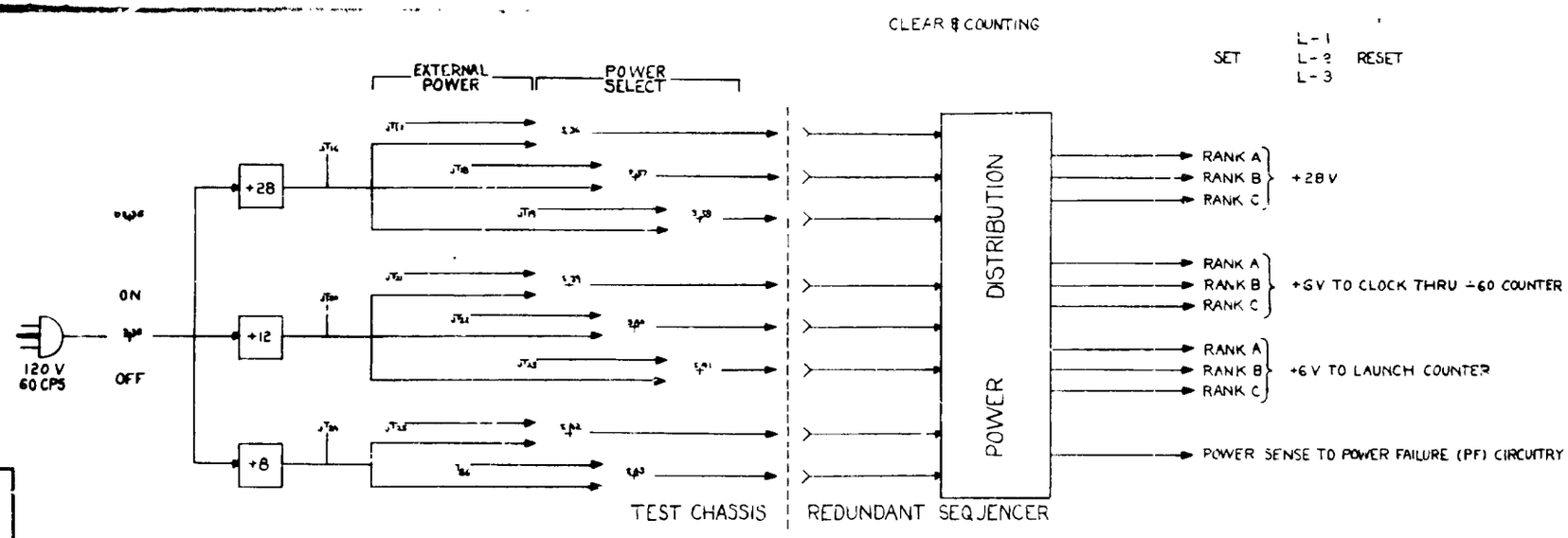
Slot Number	CARD TYPE Rank A	Rank B	Rank C
01	SPARE		
02	002		
03	004		
04	014		
05	002		
06	NS2		
07	SPACE		
08	NS3	IDENTICAL TO RANK A	IDENTICAL TO RANK A
09	NS4		
10	NS4		
11	002A		
12	NS2		
13	NS5		
14	002A		
15	NS2		
16	SPACE		
17	NS3		
18	NS4		
19	NS4		
20	002A		

APPENDIX A-11, CARD ASSIGNMENT

Slot Number	CARD TYPE Rank A	Rank B	Rank C
21	002A	↑ IDENTICAL TO RANK A	↑ IDENTICAL TO RANK A
22	46?		
23	SPACE		
24	NS6		
25	SPACE		
26	NS6		
27	SPACE		
28	NS6		
29	030		
30	SPARE		
31	NS7	002	NS7
32	NS7	004	NS7
33	NS7	NS7	NS7

REVISIONS


PROCESSORS VOTERS
DIFF DETECTOR LATCH
ON
OFF
RANK A FORCE OUTPUT
RANK B FORCE OUTPUT
RANK C FORCE OUTPUT
1
OFF
0
CLOCK
÷4
÷480
÷20
÷60
PF
1 PPM
COUNT INHIBIT
INHIBIT DISABLE
X20 SPEED-UP
CLEAR
X60 SPEED-UP
÷7
÷17
UP-DATE
UP-DATE VERIFY
UP-DATE ENABLE
MAJ L-1
MAJ L-2
MAJ L-3
1P/7 HR



A-25/26

ENGINEERING SKETCH

TITLE: FIG A-12 TEST PANEL

WESTINGHOUSE ELECTRIC CORPORATION
SURFACE DIVISION
BALTIMORE, MD., U.S.A.

SK C

SHEET 1 OF 1 SHEETS

Appendix B - Schematic Diagrams

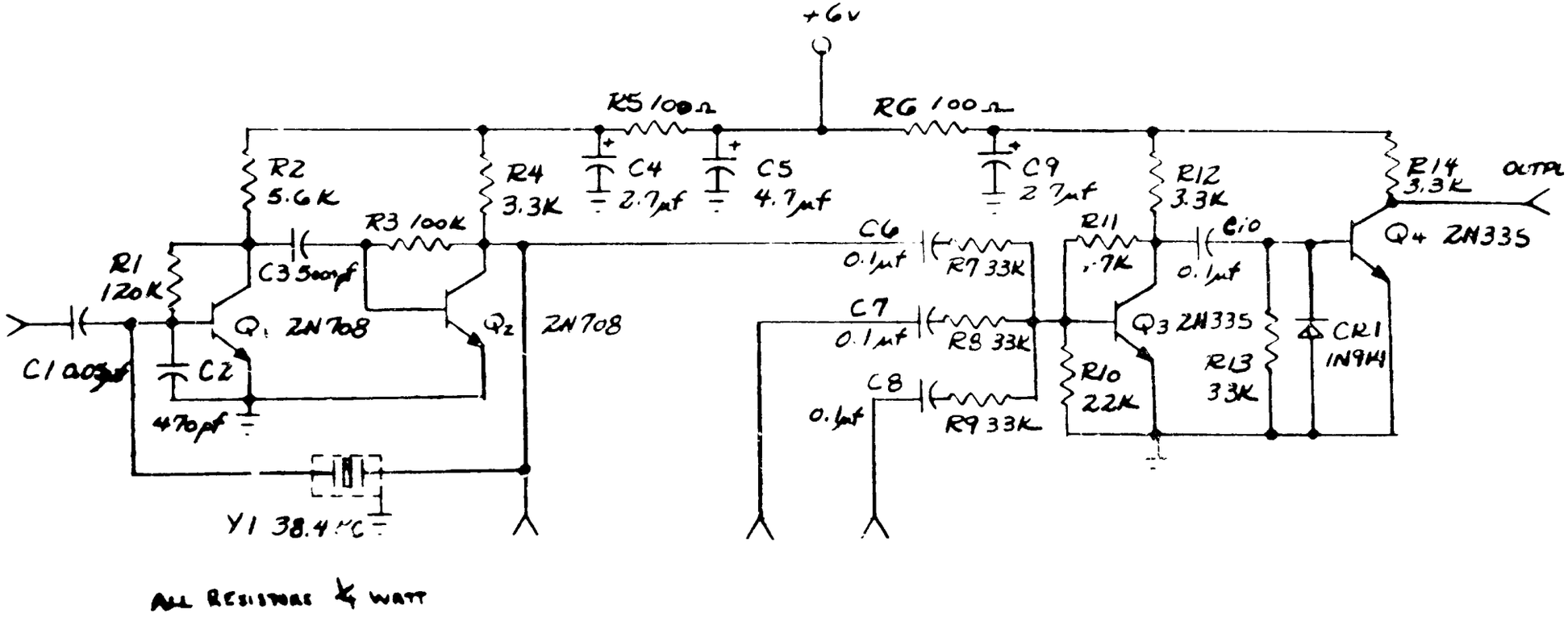
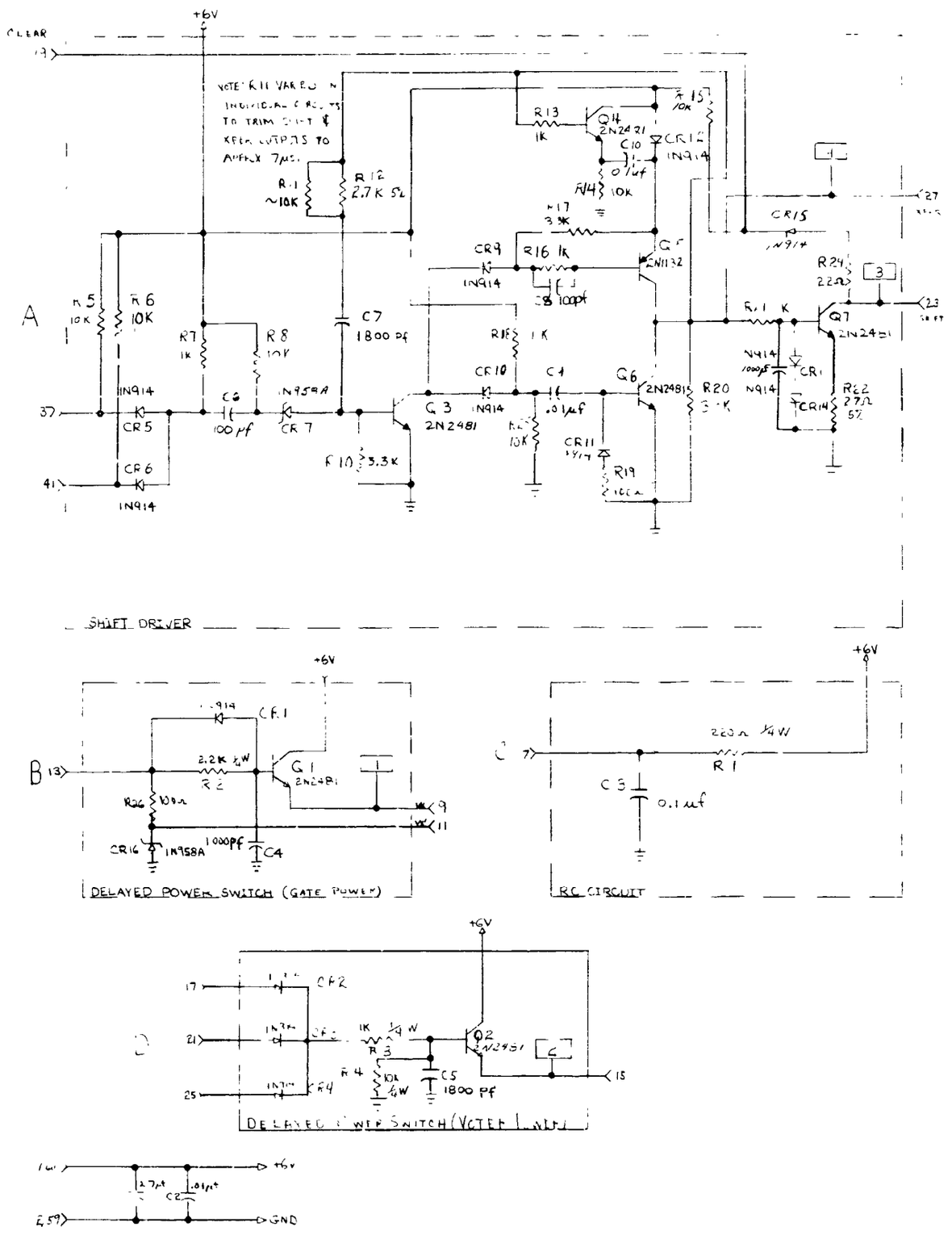


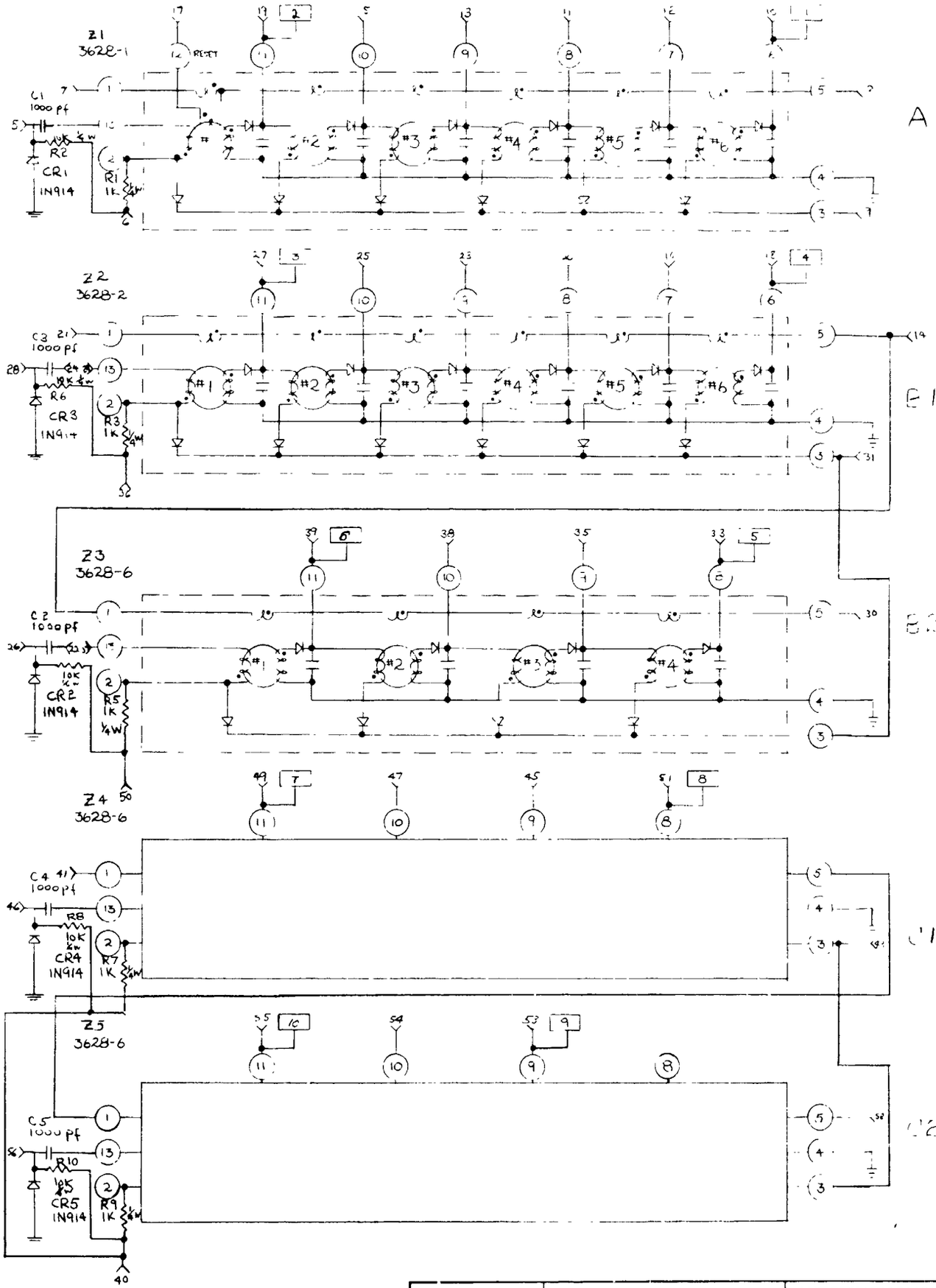
FIGURE B-1. 38.4 KHz CLOCK SOURCE (OSCILLATOR)



NOTE ALL RESISTORS 1/4 W UNLESS OTHERWISE SPECIFIED

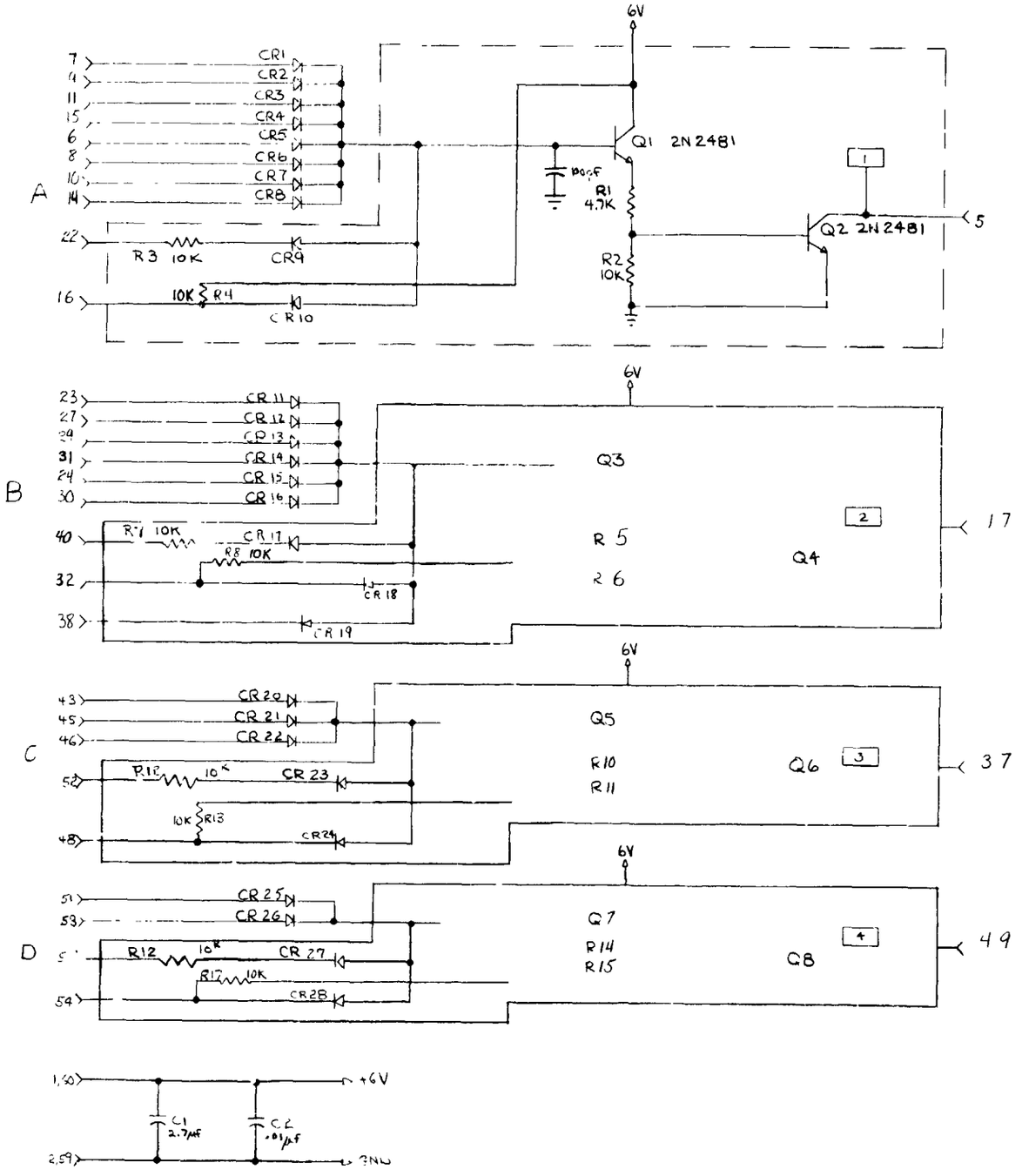
REVISIONS

ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE NS2 (33 & 333)	SURFACE DIVISION
CHARGE	SHIFT DRIVER	BALTIMORE, MD., U. S. A.
B-2	DELAYED POWER SWITCHES	NUMBER TO BE ASSIGNED TO FINAL DRAWING
	RC CIRCUIT	SK B
	FIG B-2	SHEET 1 OF 11 SHEETS



REVISIONS

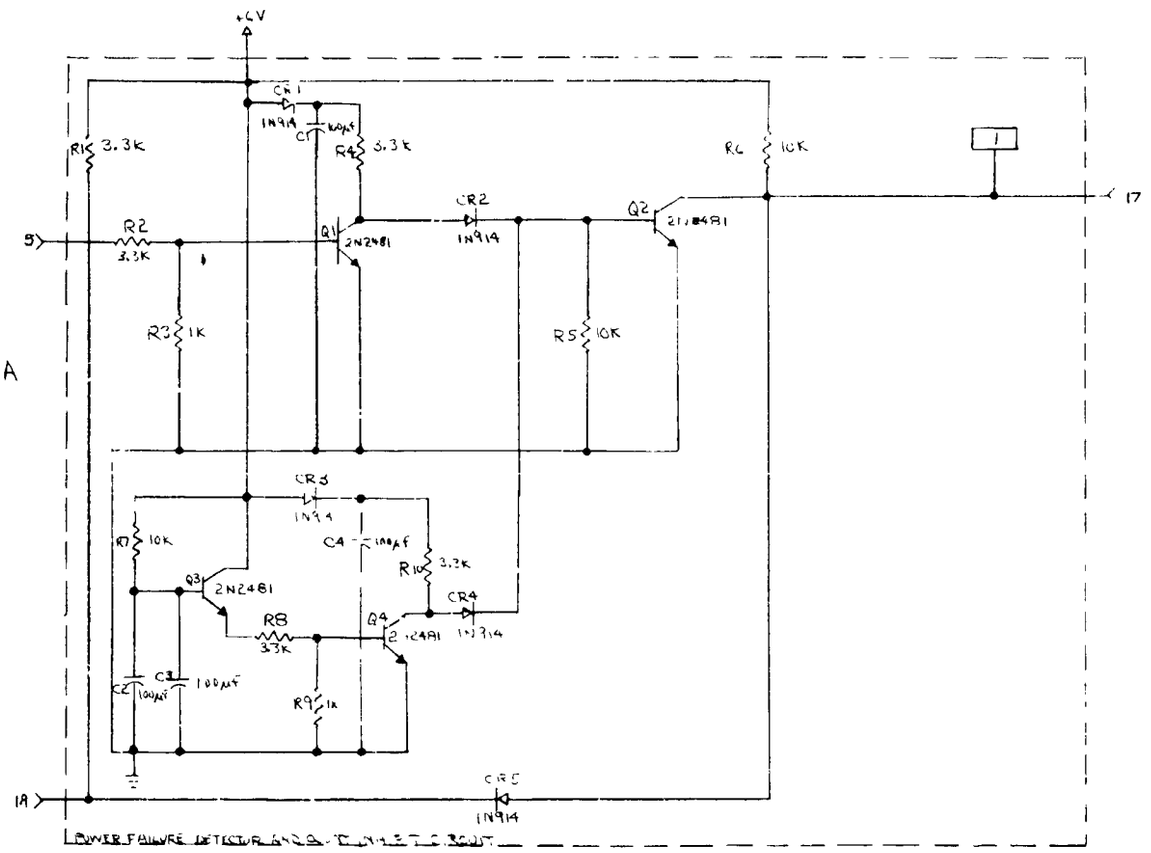
ENG	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE 3 (3328279) MAGNETIC REGISTERS	SURFACE DIVISION
CHARGE		BALTIMORE, MD U S A
B-3	FIG B-3	SK B
		SHEET 2 OF 11 SHEETS

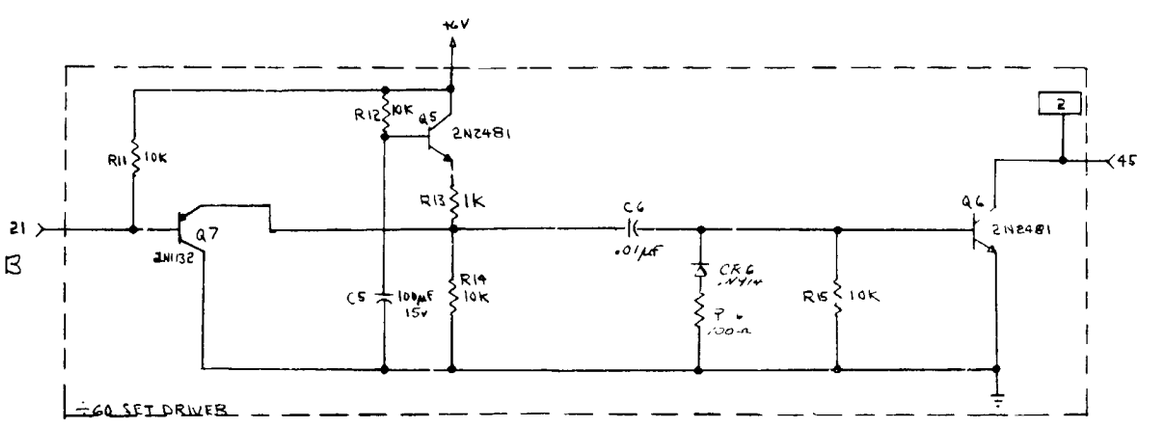


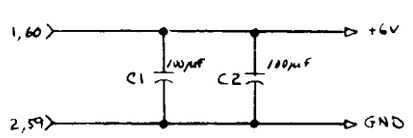
ALL RESISTORS ¼ WATT
ALL DIODES IN914

REVISIONS

ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE NS4 (3320284) BUFFERS	SURFACE DIVISION
CHARGE		BALTIMORE, MD., U. S. A.
B-4	FIG B-4	SK B
		SHEET 3 OF 11 SHEETS



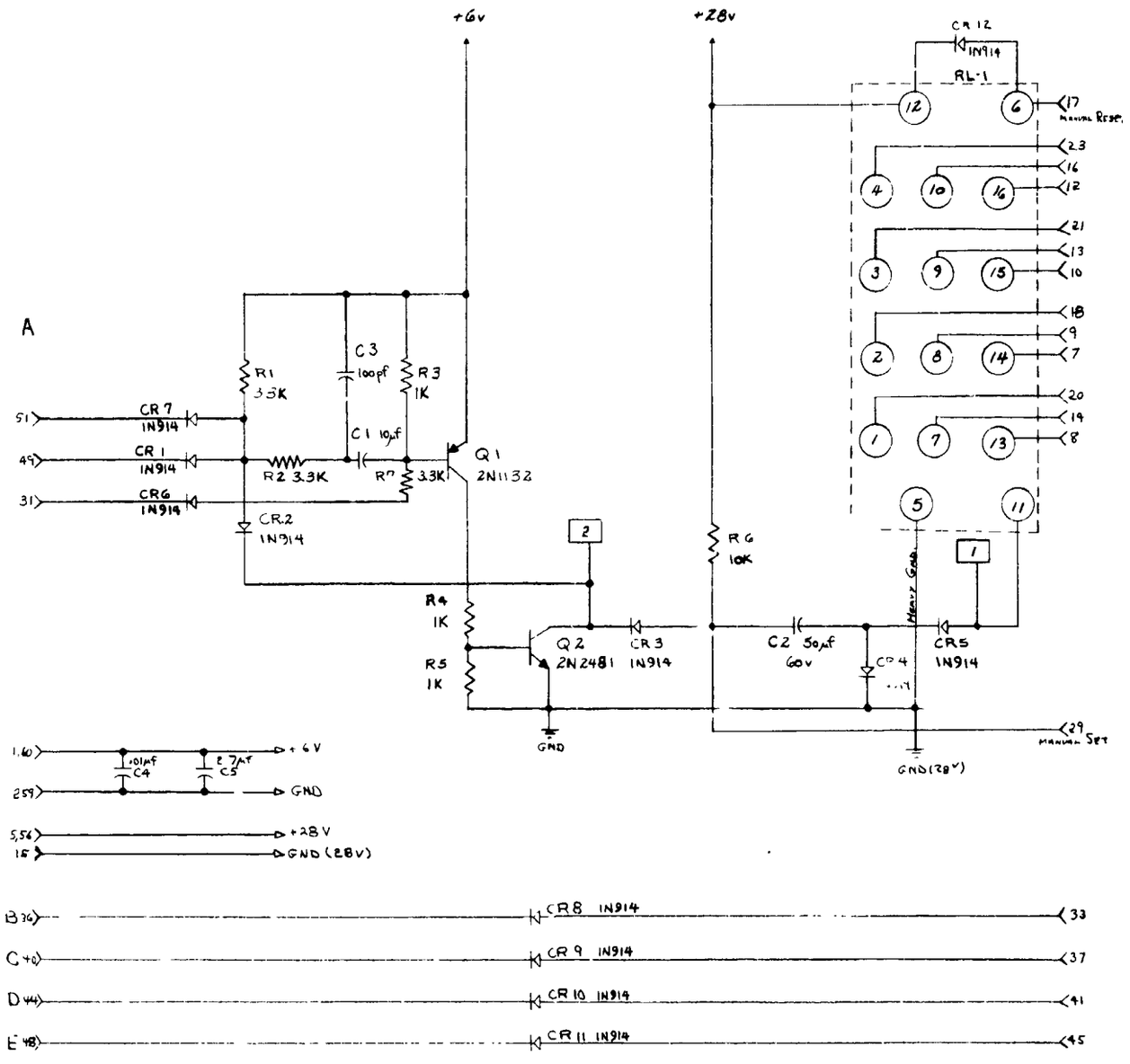




ALL RESISTORS 1/4 WATT

ENG.	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE NS5 (3320332)	SURFACE DIVISION
CHARGE	POWER FAILURE DETECTOR AND SEQUENTIAL CIRCUIT	BALTIMORE, MD., U. S. A.
B-5	-60 SET DRIVER	SK B
	FIG B-5	SHEET 4 OF 11 SHEETS

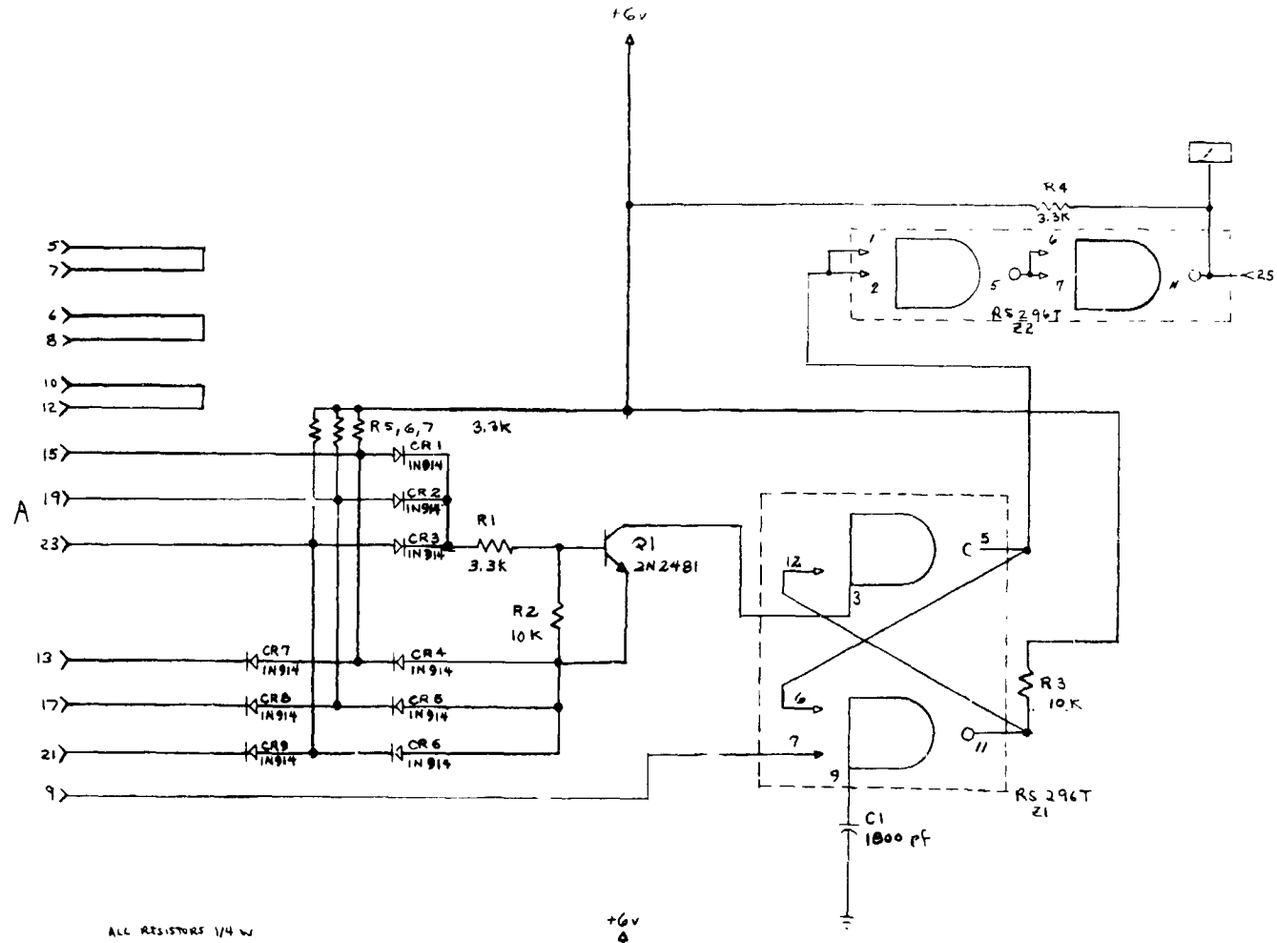
REVISIONS

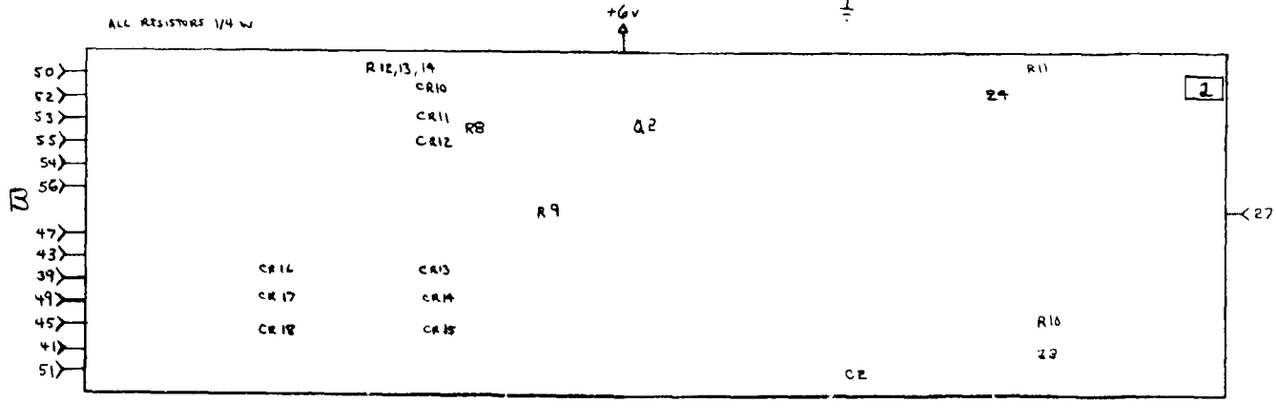


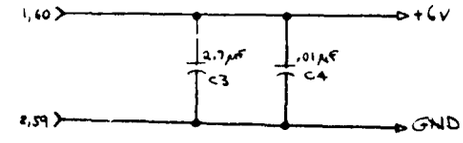
ALL RESISTORS 1/4 W UNLESS OTHERWISE SPECIFIED

REVISIONS

ENG	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	title NS6 (332D294)	SURFACE DIVISION
CHARGE	RELAY DRIVER AND DIODE ARRAY	BALTIMORE, MD., U. S. A.
B-6	FIG B-6	SK B
		SHEET 5 OF 11 SHEETS

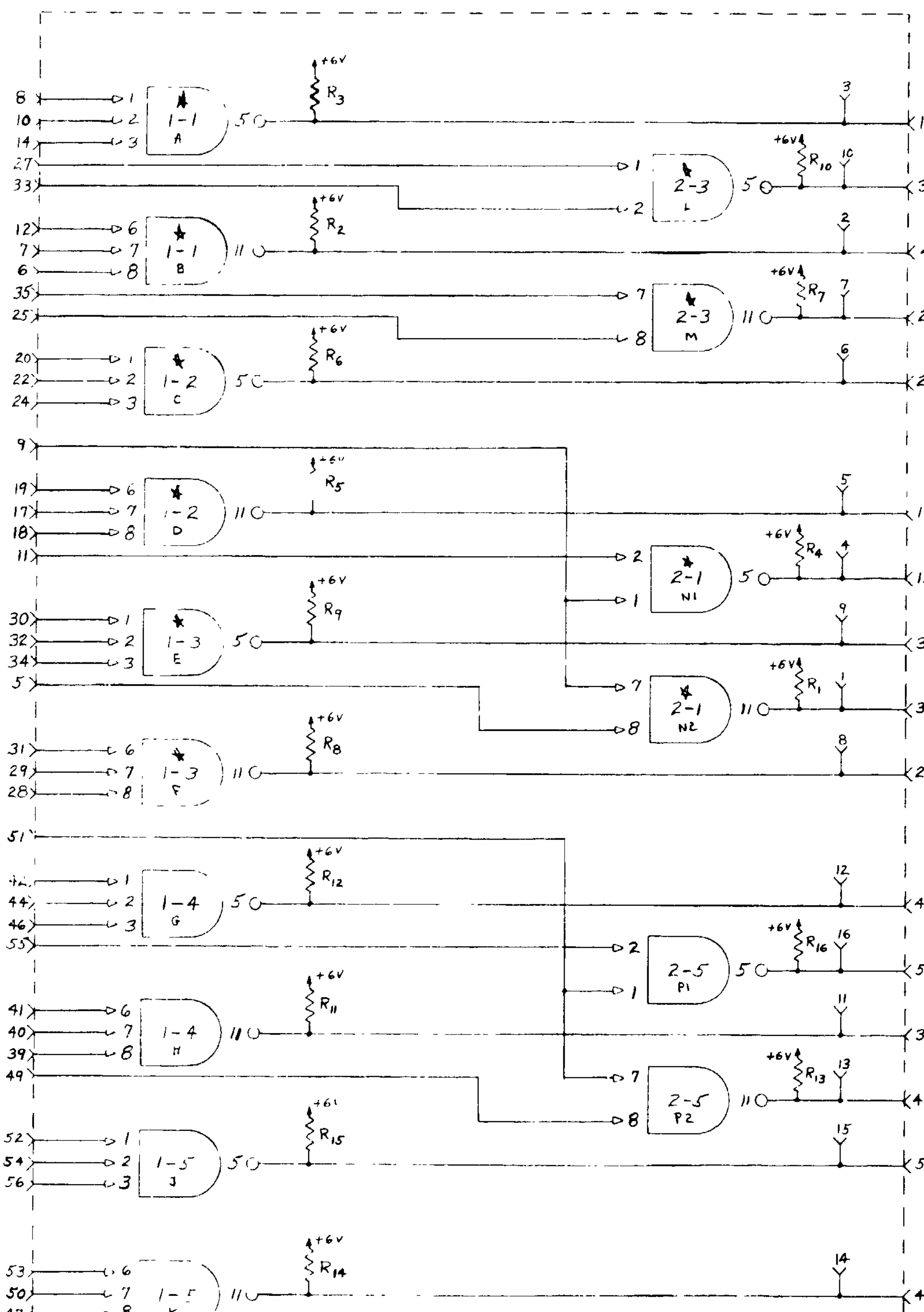


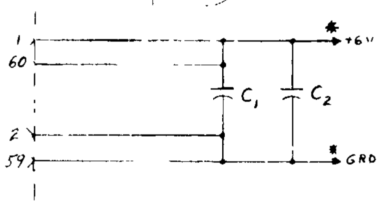




ENG	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
APPROVED	TITLE NS 7 (332D329) DIGITAL DIFFERENCE DETECTOR	SURFACE DIVISION
CHARGE		BALTIMORE, MD. U. S. A.
B-7	FIG B-7	SK B
		SHEET 6 OF 11 SHEETS

REVISIONS





* NOTE: +6V CONNECTS TO PIN #4 & GRD CONNECTS TO PIN #10 OF EACH CAN.

CANS ARE RAYTHEON RM6177 DUAL, 3-INPUT "NAND" GATES. RESISTORS ARE 10K, 1/4 WATT & C_1 IS 2.7 μfd @15V, C_2 IS .01 μfd.

NOTE: CARDS ADAPTED TO UTILIZE TWO VOLTAGES ARE CHANGED AS FOLLOWS:

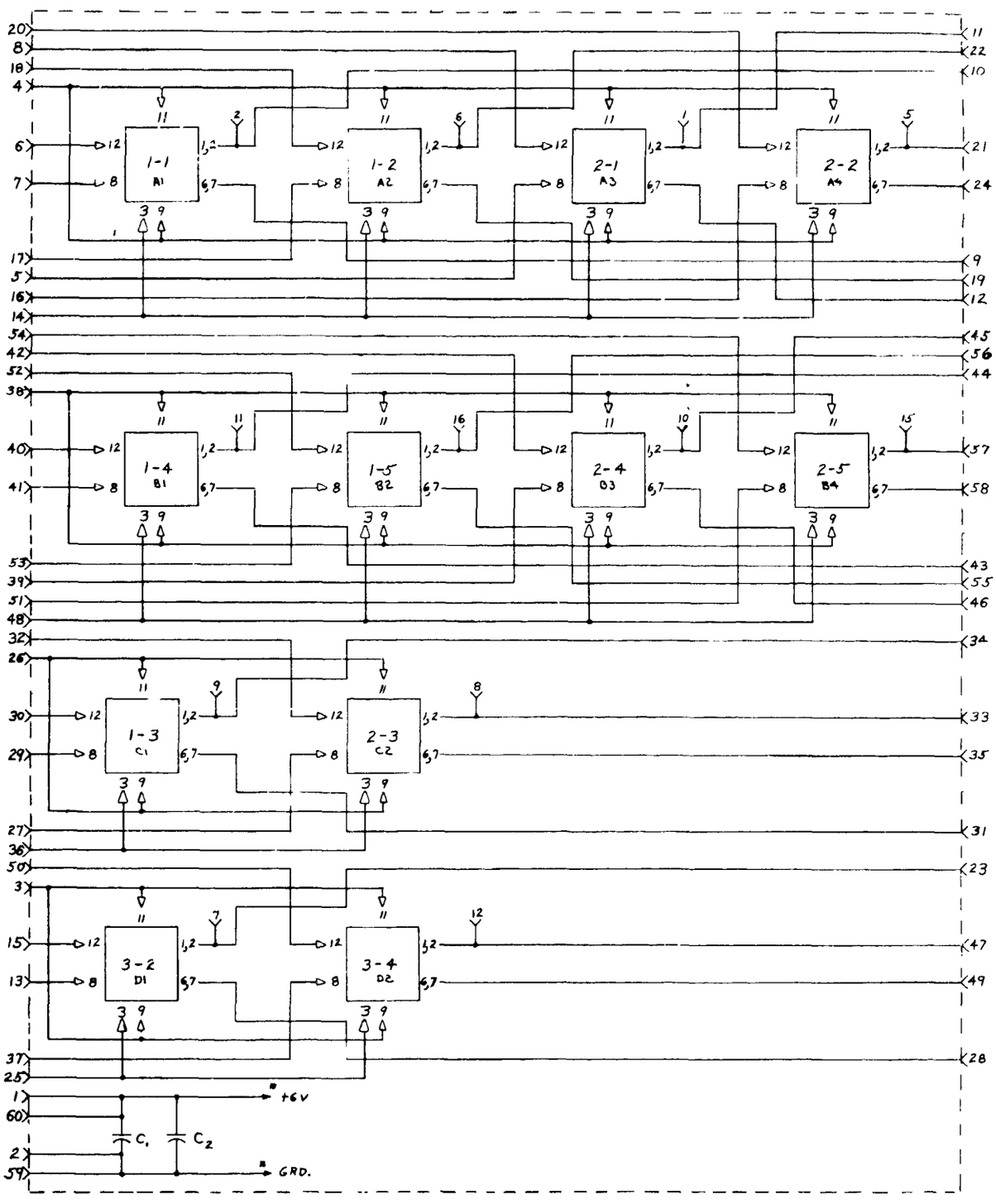
(1) ALL PULL-UP RESISTORS REMOVED
(2) FILTER CAPACITORS REMOVED.
(3) PRINTED CIRCUIT BETWEEN PIN 4 OF CANS 2-3 & 2-5 BROKEN.

CONNECTOR PIN #1 THEN FEEDS ONE-VOLTAGE TO THE GATES MARKED BY * ABOVE. PIN #60 FEEDS THE SECOND VOLTAGE TO THE UNMARKED GATES.

330D002

7/27/65 ENG. F. [illegible] APPROVED CHARGE 33518 B-8	ENGINEERING SKETCH TITLE LOGIC DIAGRAM, GATE, NAND. "002" (SINGLE VOLTAGE CARD) "002A" (CARDS ADAPTED TO UTILIZE TWO VOLTAGES) FIG B-8	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK127C[redacted]628 SHEET 7 OF 11 SHEETS

REVISIONS



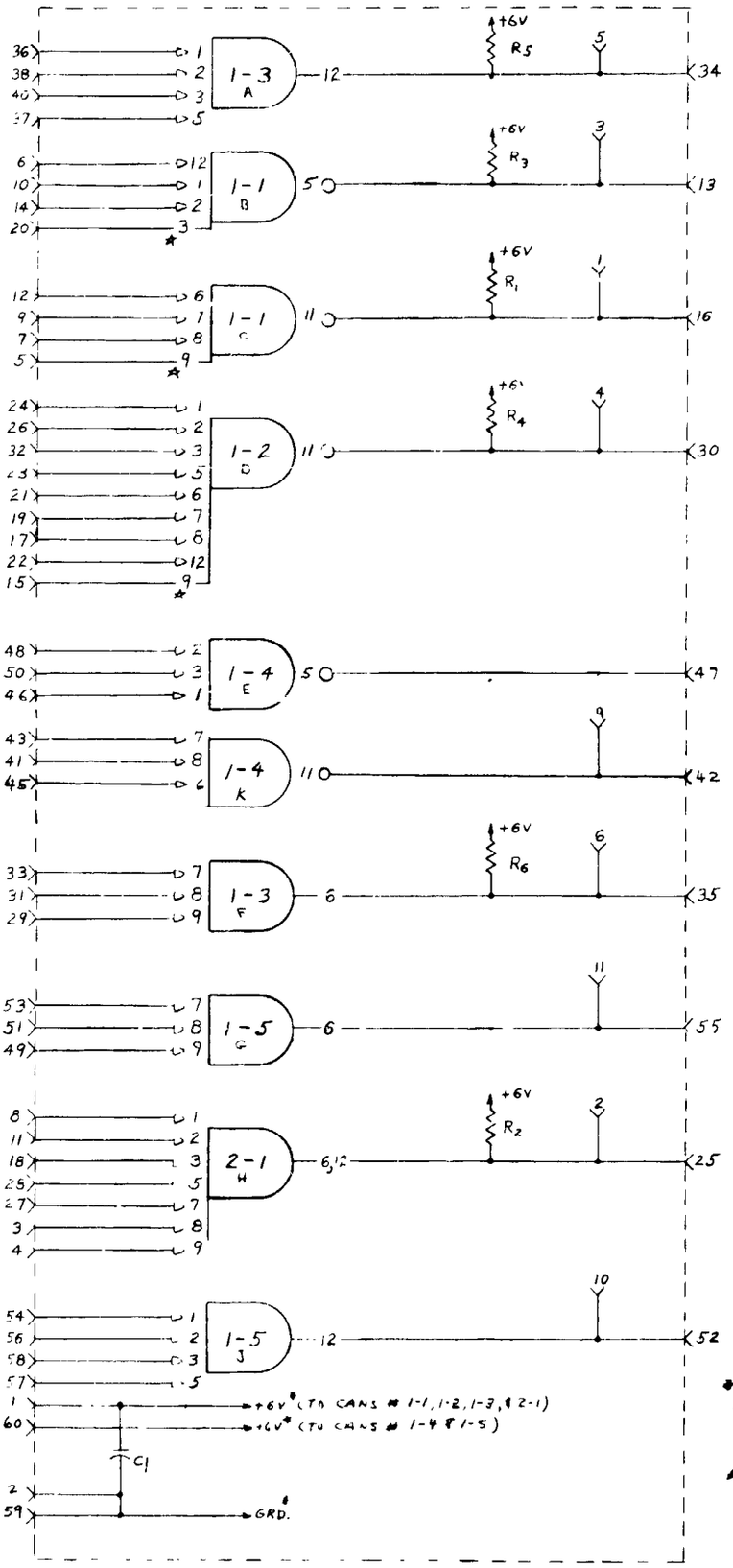
* NOTE: +6V CONNECTS TO PIN #4 & GRD CONNECTS TO PIN #10 OF EACH MED CAN.

CANS ARE RAYTHEON RSE994 J-K FLIP-FLOPS. C_1 IS 2.7 μfd @ 15V & C_2 IS .01 μfd.

330D004

7/27/65 F. Lamonte APPROVED CHARGE 33518 B-9	ENGINEERING SKETCH TITLE LOGIC DIAGRAM, REGISTER, PARALLEL. 004 FIG B-9	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD. U.S.A. SK127C629 SHEET 8 OF 11 SHEETS

REVISIONS



CAN POSITION 1-1 IS RAYTHEON RS296T. CAN POSITION 1-2 IS RS298T. & CAN POSITIONS 1-3, 1-5 & 2-1 ARE RAYTHEON RS299T. RESISTORS ARE 10K, 1/4 W & C1 IS 2.7 μfd @ 15 V, CAN POSITION 1-4 IS RAYTHEON RM6177

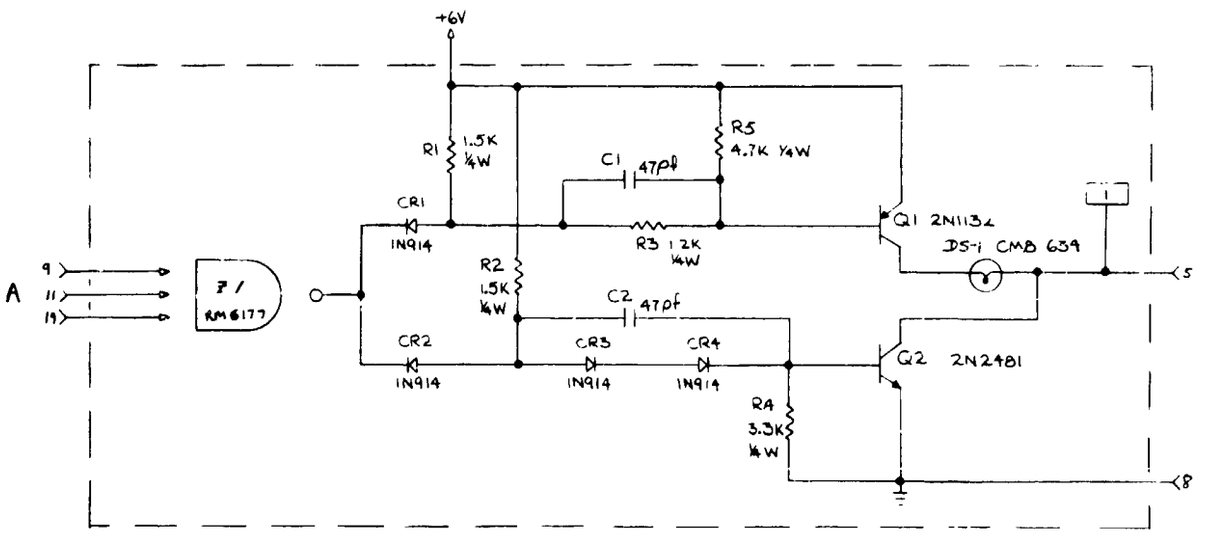
* NOTE: +6 CONNECTS TO PIN #4 & GRD CONNECTS TO PIN #10 OF EACH CAN.

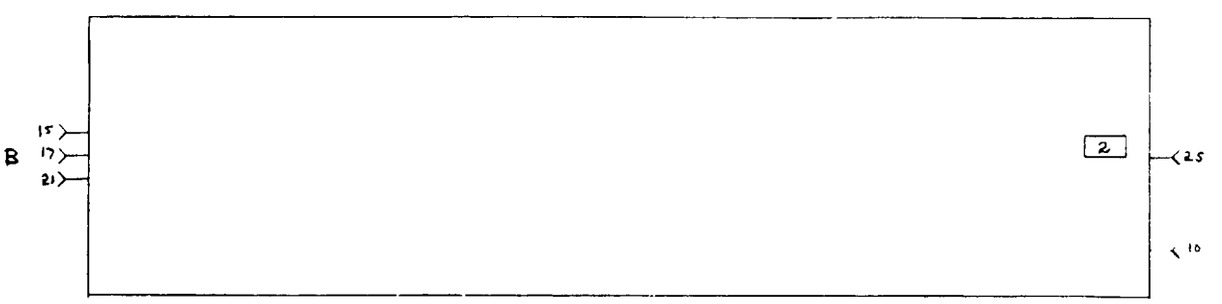
* NOTE: INPUTS TO GATES WITHOUT ARROWS DENOTE NODES.

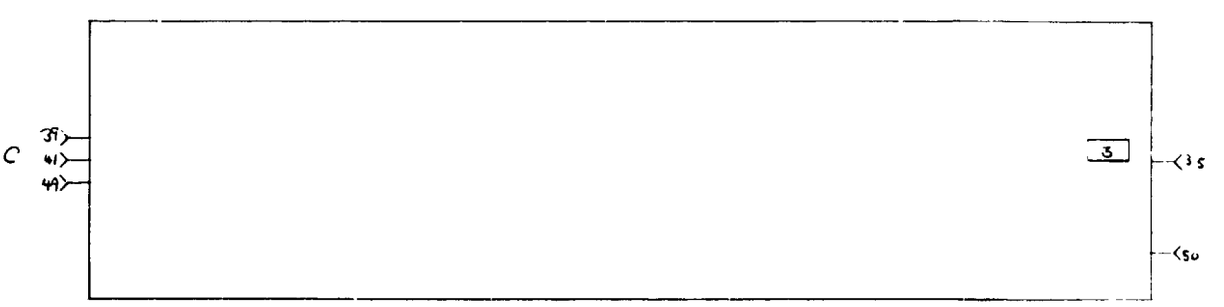
330 D 014

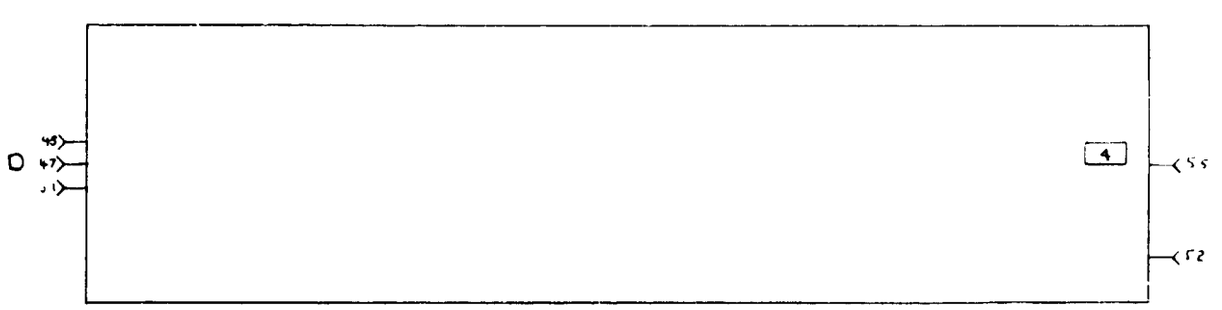
1/27/66	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION
ENG [illegible]	TITLE LOGIC DIAGRAM, GATE, FAN-IN	SURFACE DIVISION
APPROVED	014	BALTIMORE, MD., U. S. A.
CHARGE 33516		SK127C 8.01
B-10	FIG B-10	SHEET 9 OF 11 SHEETS

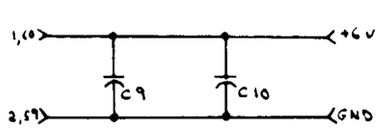
REVISIONS







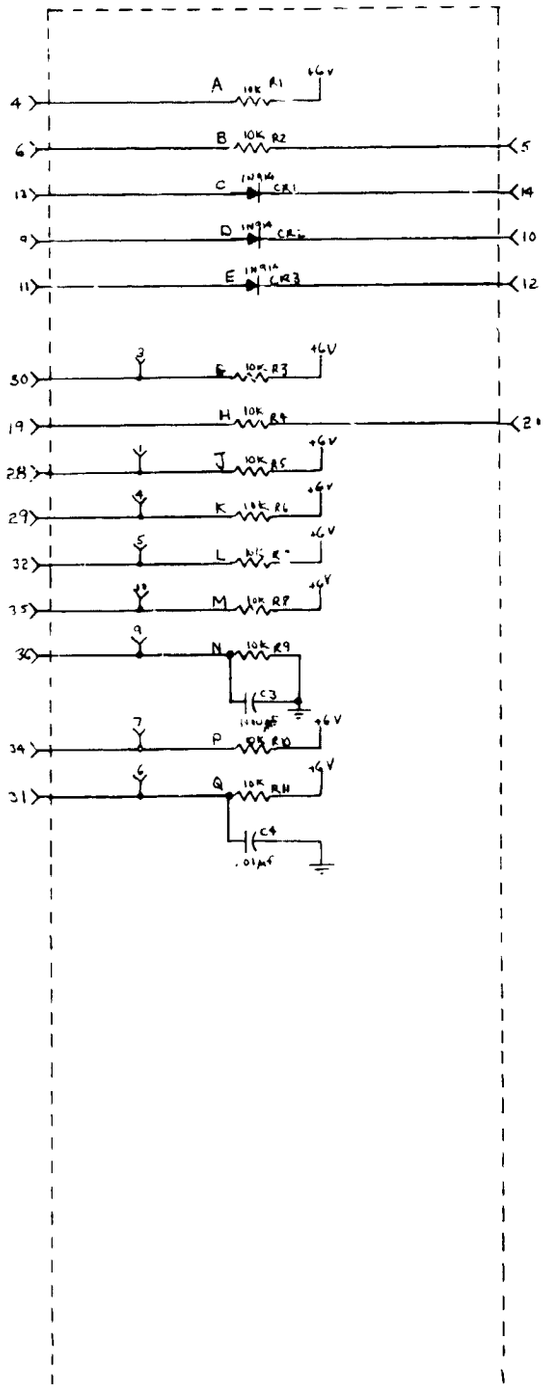


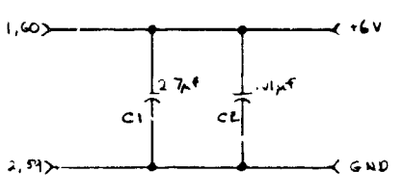


(3300469)

	ENGINEERING SKETCH TITLE 469 Positive Logic Driver	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD. U.S.A.
DWG APPROVED CHARGE B-11	Fig B-11	SK B SHEET 10 OF 11 SHEETS

REVISIONS





330070

ENG	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A.
APPROVED	TITLE 030 RESISTOR CARD	SK B
CHARGE B-12	FIG B-12	SHEET 11 OF 11 SHEETS

REVISIONS

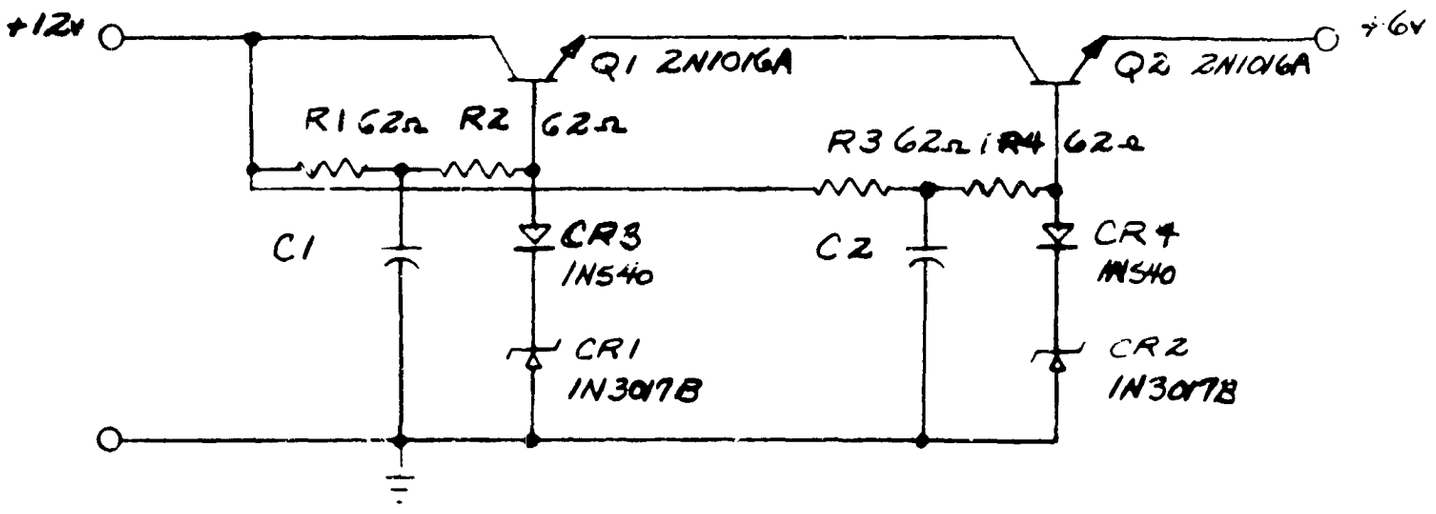
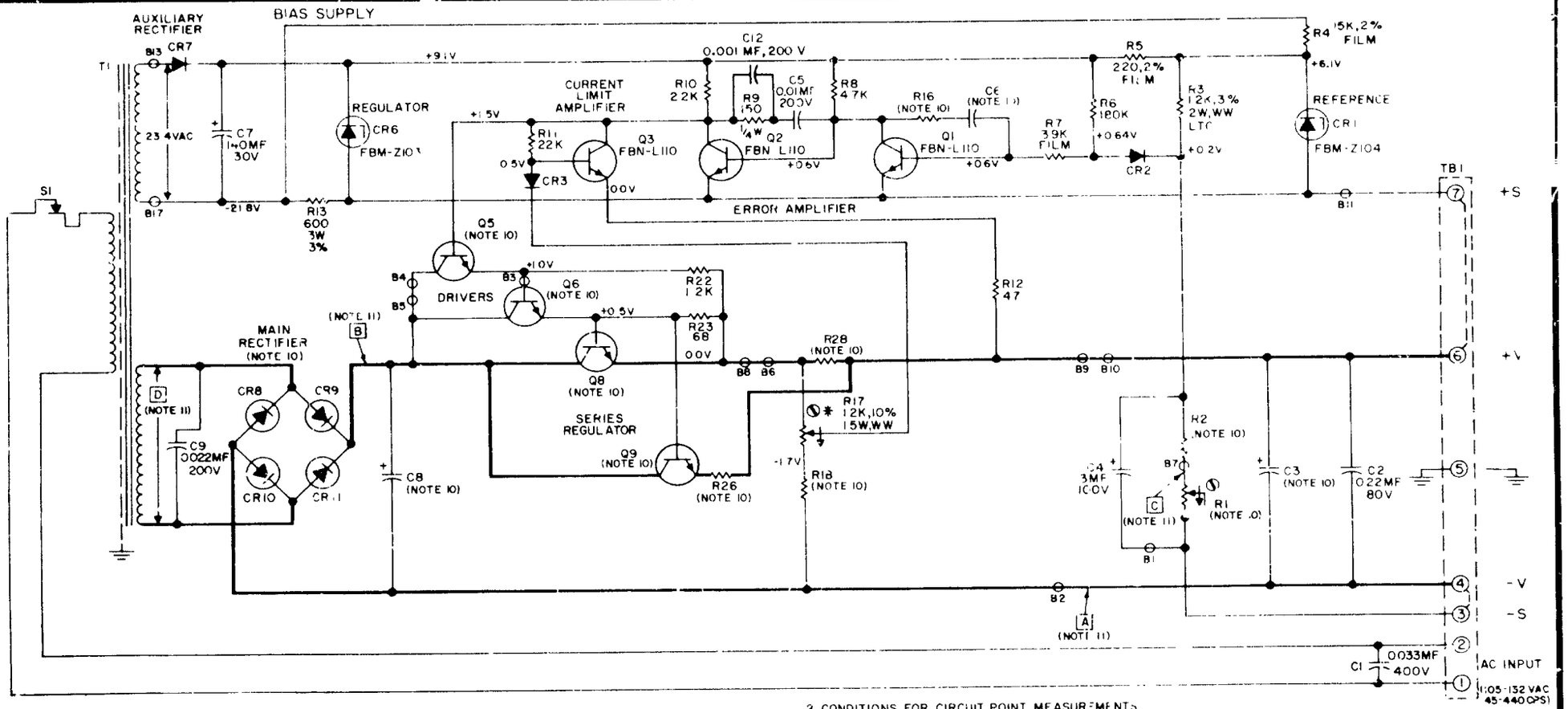


Figure B-13, Regulator



NOTES

1. RESISTOR VALUES ARE IN OHMS.
2. RESISTOR WATTAGE 1/2 WATT, RESISTORS ABOVE 2 WATTS ARE WIREWOUND UNLESS OTHERWISE NOTED
3. RESISTOR TOLERANCES: COMP. ±10%, WIREWOUND ±5%; FILM ±5%; UNLESS OTHERWISE NOTED
4. CAPACITOR TOLERANCES ELECTROLYTIC -10%,+100%, MYLAR ±10%, UNLESS OTHERWISE NOTED.
5. SYMBOLS
   - INDICATES CLOCKWISE ROTATION OF SHAFT
   - INDICATES ADJUSTMENT OR CALIBRATION CONTROL
   - INDICATES CONNECTION TO CHASSIS
   - INDICATES ACTUAL UNIT MARKING
   - SEE INSTRUCTION MANUAL
   - LAMBDA PT #FBL-00-030 USE IN4002 DIODE FOR REPLACEMENT UNLESS OTHERWISE NOTED.
   - INDICATES TERMINAL ON PRINTED WIRING BOARD "B"
6. DESIGNATIONS ARE LAMBDA PART NUMBERS.
7. DERATE CURRENT 10% FOR 45-55 CPS OR 360-440 CPS
8. CONDITIONS FOR CIRCUIT POINT MEASUREMENTS INPUT 115VAC, 60CPS, OUTPUT NOM'L VDC, NO LOAD INDICATED VOLTAGES ARE TYPICAL VALUES AND ARE DC UNLESS OTHERWISE NOTED DC MEASUREMENTS TAKEN WITH 20,000 OHMS/V VOLTMETER BETWEEN +S (TERM 7) & INDICATED POINTS UNLESS NOTED.
9. COAT BOTH SIDES OF INSULATING WAFER WITH DOW CORNING NO 340 SILICONE GREASE
10. SEE TABLE I FOR COMPONENT VALUES
11. SEE TABLE I FOR VOLTAGE VALUES
12. IF Q5 IS REPLACED, ALWAYS RETAIN RADIATOR AND INSTALL WITH NEW TRANSISTOR.

REFERENCE DESIGNATIONS NOT USED	
Q7	R14
Q4	R15
CR4,5	R24
R19-R21	R25
	R27

MODELS	MODELS
LM-06	LM-060
LM-C8	LM-C84
LM-C10	LM-C26
LM-C12	LM-060
LM-C15	LM-C15
LM-C18	

FOR WIRING OF POWER SUPPLY TO LOAD REFER TO SUPPLY TO-LOAD WIRING DIAGRAMS

DOTTED CONNECTIONS SHOWN ON TB1 INDICATE JUMPERS IN PLACE FOR LOCAL SENSING CONNECTION

THIS SCHEMATIC APPLIES TO UNITS BEARING SERIAL NO PREFIXES A C

SCHEMATIC DIAGRAM
REGULATED POWER SUPPLY
LM-C12

Figure B-14

LAMBDA
ELECTRONICS CORP.
MELVILLE NEW YORK

B-14

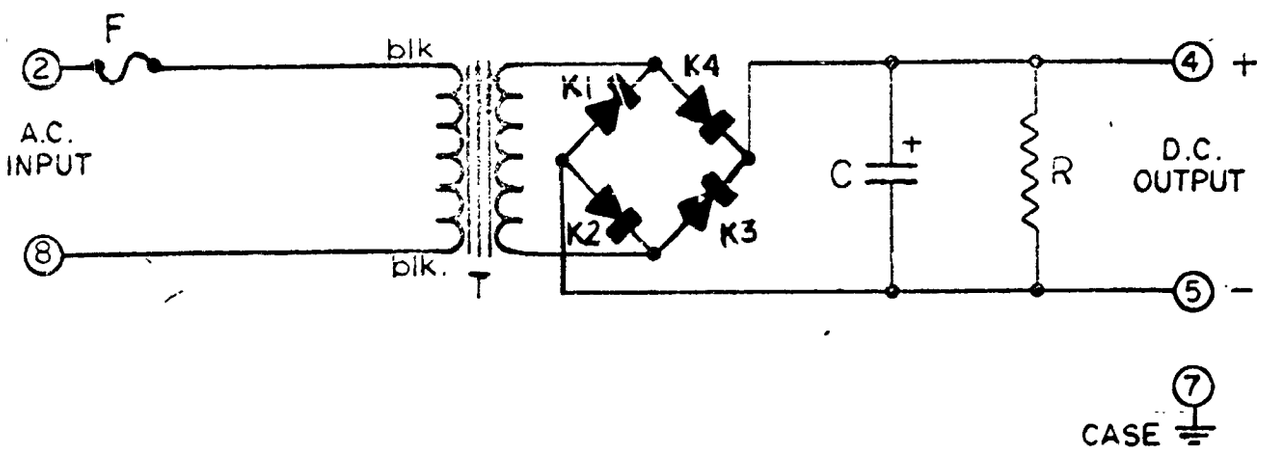
B-15

TABLE I

DATA REFERENCES FOR MODELS LM-C8 — LM-C48

Model	Voltage Range (VDC)	Max. Current (Amperes)				Schematic Voltage Measurement				Schematic Components									
		40°C	50°C	60°C	71°C	A VDC	B VDC	C VDC	D VAC	C3	C6	C8	CR 8-11 (FBL 00-)	Q5 (FBN-)	Q6 (FBN-)	Q8, Q9 (FBN-)	R1 5% 5W	R2 5% 3W	R16 10% 1/2W	R13 5% 1/2W	R26, R28
LM-C8	8±5%	4.4	3.8	3.0	2.0	-8.0	+21.2	-6.12	20.7	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	36486	36485	1K	1.2K	820	2.4K	0 39 ±5%, 5W
LM-C9	9±5%	4.2	3.6	3.0	2.0	-9.0	+21.1	-6.12	21.2	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	36486	36485	1K	1.2K	820	2.4K	0 56 ±5%, 5W
LM-C10	10±5%	4.0	3.5	2.9	2.0	-10.0	+21 7	-6.12	22.4	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	36486	36485	2.2K	1 2K	820	2.4K	0 56 ±5%, 5W
LM-C12	12±5%	3.8	3.3	2.8	2.0	-12.0	+23.2	-9 18	24.9	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	36486	36485	2.2K	1.8K	820	2 4K	0 68 ±5%, 5W
LM-C15	15±5%	3.4	3.2	2.7	1.8	-15.0	+23.6	-9.18	27.3	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	35469	36220	2 2K	1.8K	820	2 4K	0 68 ±5%, 5W
LM-C18	18±5%	3.0	2.8	2.5	1.7	-18.0	+24.5	-12.75	30.0	900 MF, 35V	0.018 MF, 200V	3,000 MF, 35V	046	L109	35469	36220	2.2K	2.5K	820	6.8K	0 68 ±5%, 5W
LM-C20	20±5%	2.9	2.7	2.4	1.7	-20.0	+26.5	-12.75	32.9	500 MF, 30V	0.018 MF, 200V	1,520 MF, 60V	049	L109	36488	36487	2.2K	2.5K	820	6 8K	0.75 ±5%, 5W
LM-C24	24±5%	2.5	2.4	2.2	1.5	-24.0	+32.1	-18.4	39.7	500 MF, 60V	0.018 MF, 200V	1,520 MF, 60V	049	L109	36488	36487	2.2K	3.6K	820	6.8K	1.0 ±3%, 5W
LM-C28	28±5%	2.3	2.1	2.0	1.4	-28.0	+31.7	-22.9	42.2	500 MF, 60V	0.018 MF, 200V	1,520 MF, 60V	049	L109	36488	36487	2.2K	4.5K	820	6.8K	1 25 ±3%, 3W
LM-C36	36±5%	2.0	1.8	1.7	1.3	-36.0	+34 6	-28.6	50.0	500 MF, 60V	0.018 MF, 200V	1,520 MF, 60V	049	L108	36488	36487	3.3K	5 6K	820	10.0K	1 25 ±3%, 3W
LM-C48	48±5%	1.6	1.4	1.3	1.0	-48.0	+52.0	-40 8	70.7	200 MF, 100V	0.01 MF, 200V	580 MF, 100V	038	L108	35903	35902	3.3K	8 0K	3 9K	10.0K	1 5 ±3%, 3W

Figure B-14, +12 Volt Regulated Power Supply (Con'T)



F - 1/2 Amp. Slow-Blow

C - 1000 MFD 50 Volts

R - 150 ohm 10 Watt

K1, 2, 3 & 4 - 1N1218

T - # US-24V xfmr. secondary taps: RED & YELLOW

Figure B-15, +28-Volt Power Supply

Appendix C - Assembly Drawings and Parts Lists

BLANK PAGE

FIGURE C-1. PARTS LIST, 38.4 KHz CLOCK (OSCILLATOR)

QUANTITY REQUIRED*	PART NUMBER	DESCRIPTION
1	RC07GF124K	Resistor R1
1	RC07GF562K	Resistor R2
1	RC07GFN104K	Resistor R3
3	RC07GF332K	Resistor R4, R12, R14
2	RC07GF101K	Resistor R5, R6
4	RC07GF333K	Resistor R7-R9, R13
1	RC07GF223K	Resistor R10
-	CS13AD475K	Capacitor C5
2	CS13AD275K	Capacitor C4, C9
1	0.05 uf	Capacitor, Ceramic Disc C1
4	0.01 uf	Capacitor, Ceramic Disc C6-C8, C10
1	470 pf	Capacitor, Dura Mica C2
1	5000 pf	Capacitor, Dura Mica C3
1	1N914	Diode
2	2N335	Transistor Q3, Q4
2	2N708	Transistor Q1, Q2
1	13NS	Crystal, Reeves, Hoffman, 38.4 KC, Y1
1	#8000-DG1	Crystal Socket Assembly, Augat
1		Terminal Block, 3 point

* For one of the three Clock Circuits used.

ORIGINAL DATE OF DWG 15 APR 66	APPD	
DRAFTSMAN JOHNSON	CHECKED McCauley	APPD M. Pitt
	SPECIFICATION	TYPE-MOD-SERIES
GOVT		
CONTR		
CONTRACT NO		

Westinghouse Electric Corporation
DEFENSE AND SPACE CENTER — BALTIMORE MARYLAND 21203 U S A

DESIGN ACTIVITY APPROVAL

PROCURING ACTIVITY APPROVAL

PARTS LIST

89661 PL 332D336G01 A

CODE IDENT | SHEET 1 OF 3 SHEETS | REV

ITEM NOMENCLATURE

PRINTED WIRING ASSEMBLY
SHIFT DRIVER
N S E

APPLICATION						LTR	REVISION DESCRIPTION	DATE	APPD
ASSY IDENT NO	QTY. REQD. NEXT ASSY	QTY. REQD. FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	USED ON SERIAL NO. FROM	USED ON SERIAL NO. THRU			
							A PARTS LIST RELEASED	5-2-66	

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
-	-	A													

QTY REQUIRED G01	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO.
X		332D336		ASSEMBLY 1 THRU 4		1
1		332D335H01		PRINTED WIRING BOARD		2
X				TEST SPECIFICATION		3
X				SCHEMATIC		4
2		331C264H34	V	EYELET		5
~~1~~		~~[illegible]~~	~~V~~	~~INSULATOR, DISK~~		6
~~1~~		~~[illegible]~~	~~V~~	~~INSULATOR, DISK~~		7
1		CS13BD275K		CAPACITOR C1	MIL-C-26655	8
2		788C016H01	V	CAPACITOR C2, C9		9
2		332D342H05	V	CAPACITOR C3, C10		10
2		CK05CW102K		CAPACITOR C4, C11	MIL-C-11015	11
2		332D342H06	V	CAPACITOR C5, C7		12
2		CK05CW101K		CAPACITOR C6, C8	MIL-C-11015	13
13		1N914		DIODE CR1 TO CR6, CR9 TO CR15	MIL-S-19500/116A	14
2		1N958A		DIODE CR7, CR16	MIL-S-19500/117	15
6		2N2481		TRANSISTOR Q1 TO Q4, Q5, Q7	MIL-S-19500/268A	16

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

FORM NO BA 5389-1

89661	PL332D3[illegible]G01	A
CODE IDENT	SHEET 2 OF 3 SHEETS	REV

QTY REQUIRED G01	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO
1		2N1132		TRANSISTOR Q5	MIL-S-19500/177	17
1		RC07GF221K		RESISTOR R1	MIL-R-11	18
1		RC07GF222J		RESISTOR R2	MIL-R-11	19
6		RC07GF102K		RESISTOR R3, R7, P13, R16, R18, R21	MIL-R-11	20
8		RC07GF103K		RESISTOR 5	MIL-R-11	21
3		RC07GF332K		RESISTOR R10, R17, R20	MIL-R-11	22
1		RC07GF272J		RESISTOR R12	MIL-R-11	23
2		RC07GF101K		RESISTOR R19, R26	MIL-R-11	24
1		RC2CGF2R7J		RESISTOR R22	MIL-R-11	25
1		RC07GF220K		RESISTOR R24	MIL-R-11	26
X		161P769		PRINTED WIRING MASTER		27

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

FORM NO 8A 5308-2

NOTES

(1) ORDER PURCHASED PARTS TO COMPLY WITH T-673303

(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP 12 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

(3) DIP SOLDER PER PS 291944-1

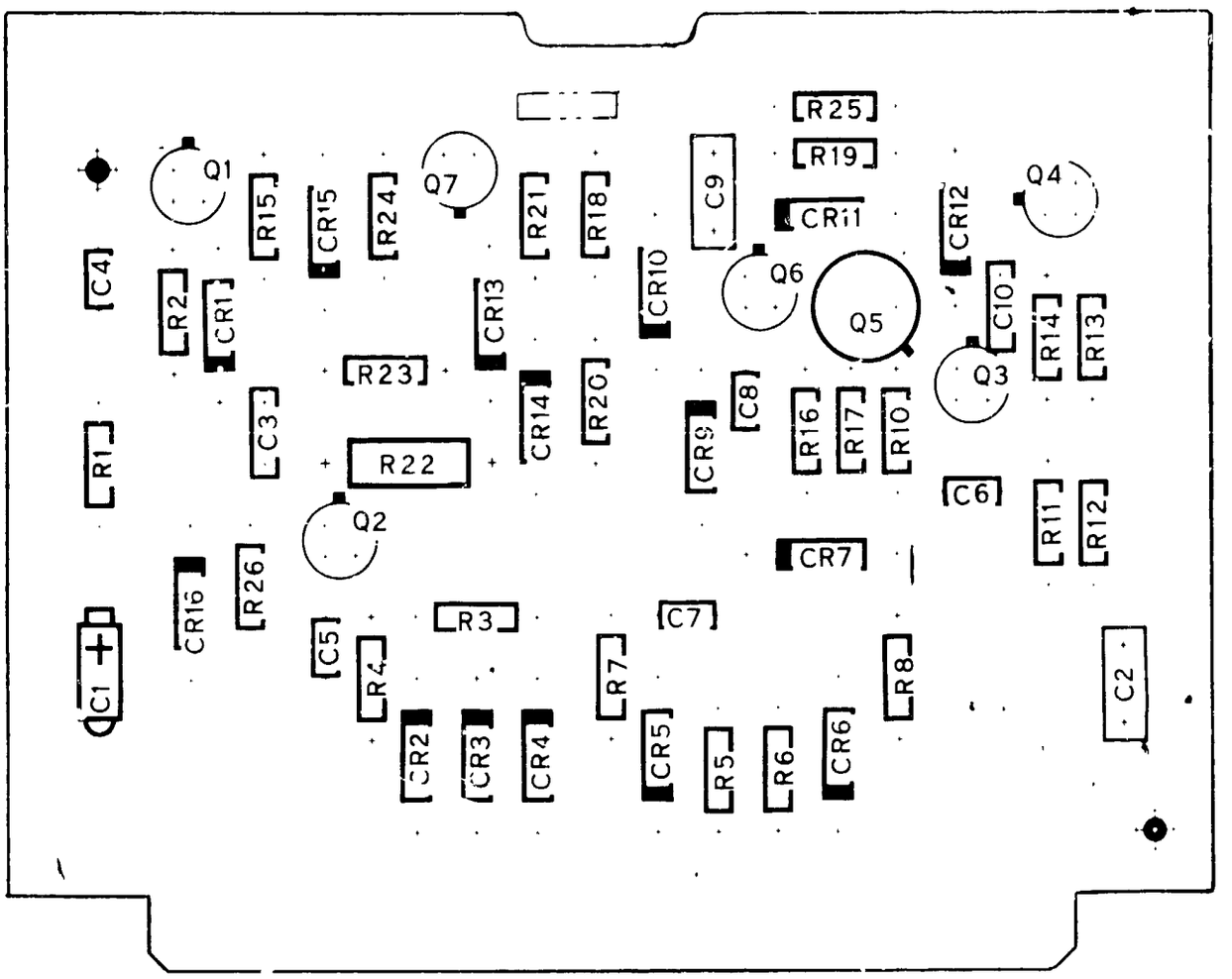
(4) FOR MIL EQUIVALENTS SEE DWG 385A000

(5) R4, R5, R6, R8, R11, R14, R15, R25

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	DWG RELEASED DSGN SPEC 732032		

C-4

CODE IDENT NO	SIZE	DWG NO
89661	B	P332033660 1
SCALE		SHEET 3



Westinghouse Electric Corporation		
DEFENSE CENTER (12) BALTIMORE MD., U. S. A.		
TITLE PRINTED WIRING ASSEMBLY SHIFT DRIVER N S 2		
CODE IDENT NO.	SIZE	DWG NO.
89661	D	3320336

ORIGINAL DATE OF DWG 12 APR 66	APPD	**Westinghouse Electric Corporation**	**PARTS LIST** 89661 PL 332D279G01 A
DRAFTSMAN R. WALIK	CHECKED McCaulley	APPD	DEFENSE AND SPACE CENTER (W) BALTIMORE MARYLAND 21203 U.S.A.	CODE IDENT	SHEET 1 OF 2 SHEETS	REV
	SPECIFICATION	TYPE-MOD-SERIES		ITEM NOMENCLATURE
GOVT			DESIGN ACTIVITY APPROVAL	PRINTED WIRING ASSY MAGNET C REGISTER N.S.3
CONTR			PROCURING ACTIVITY APPROVAL	
CONTRACT NO				

APPLICATION

ASSY IDENT NO	QTY REQD NEXT ASSY	QTY REQD FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	USED ON SERIAL NO. FROM	USED ON SERIAL NO. THRU
				38552		

LTR	REVISION DESCRIPTION	DATE	APPD
A	DWG RELEASED	[illegible]	

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	A														

QTY REQUIRED -01	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO
X		332D279		ASSEMBLY (1)	[illegible]	1
1		332D278H01		PRINTED WIRING BOARD		2
X				LOGIC DIAGRAM		3
X				TEST SPEC		4
2		331C264H34	V	EYELET		5
5		CK05C./102K		CAPACITOR - C1 TO C5	MIL-C-11015	6
5		1N914		DIODE CR1 - CR5	MIL-S-19500/1164	7
5		RC07GF102K		RESISTOR R1,R3,R5,R7,R9	MIL-R-11	8
5		RC07GF103K		RESISTOR R2,R4,R6,R8,R10	MIL-R-11	
1		332D342H01	V	MAGNETIC REGISTER Z1		10
1		332D342H02	V	MAGNETIC REGISTER Z2		11
3		332D342H03	V	MAGNETIC REGISTER Z3,Z4,Z5		12

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

FORM NO. BA 5188

WR-12/A1

PR

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	DWG RELEASED D SPEC 732029		

NOTES

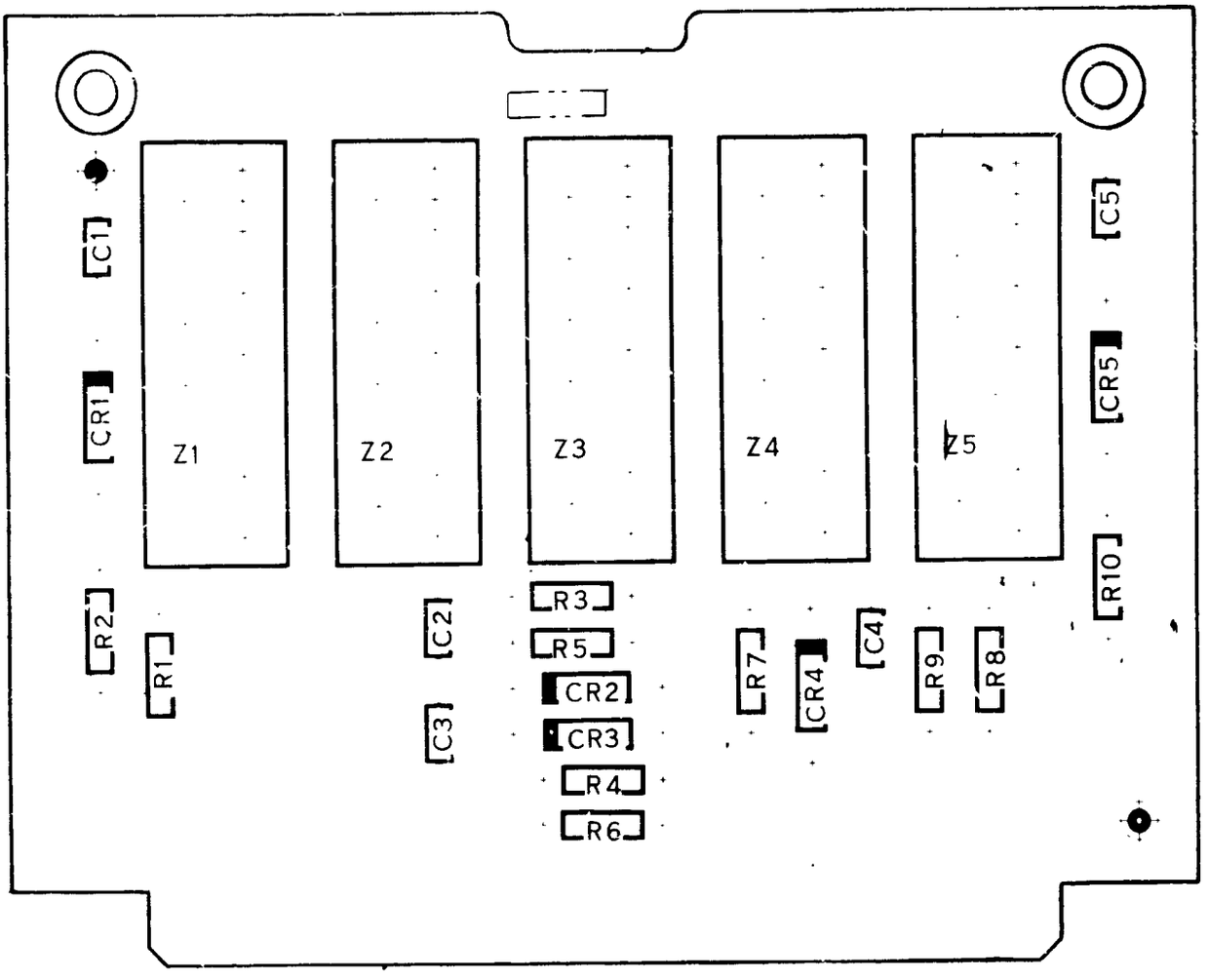
(1) ORDER PURCHASED PARTS TO COMPLY WITH T-673303

(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP 12 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

3 · DIP SOLDER PER PS 291944-1

(4) FOR MIL EQUIVALENTS SEE DWG 385A000

CODE IDENT NO	SIZE	DWG NO
89661	B	PL332D279G01
SCALE ~		SHEET 2



Westinghouse Electric Corporation		
DEFENSE CENTER ⓦ BALTIMORE MD., U. S. A.		
TITLE PRINTED WIRING ASSEMBLY MAGNETIC REGISTER		
CODE IDENT NO.	SIZE	DWG NO.
89661	D	3320279

ORIGINAL DATE OF DWG	APPD	Westinghouse Electric Corporation	PARTS LIST
DRAFTSMAN R. Walk	CHECKED E.W. Eggers	APPD	89661 PL 332284 G01 A
	SPECIFICATION	TYPE-600-SERIES	CODE IDENT / SHEET 1 OF 2 SHEETS / REV
GOVT			DEFENSE AND SPACE CENTER — BALTIMORE MARYLAND 21203 U S A
CONTR			DESIGN ACTIVITY APPROVAL
CONTRACT NO			PROCURING ACTIVITY APPROVAL

ITEM NOMENCLATURE: PRINTED WIRING ASSY NS4 - BUFFERS

APPLICATION						LTR	REVISION DESCRIPTION	DATE	APPD
ASSY IDENT NO.	QTY. REQD NEXT ASSY	QTY. REQD FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	USED ON SERIAL NO. FROM	USED ON SERIAL NO. THRU			
				38552			A DRAWING RELEASED	4-18-66	

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	B														

QTY REQUIRED G01	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO
X		332D284		ASSEMBLY (1)	(2) (3) (4)	1
1		332D283H01		PRINTED WIRING BOARD		2
X				LOGIC DIAGRAM		3
X				TEST SPEC		4
2		331C264H34	V	EYELET		5
1		CS13BD275K		CAPACITOR, C1	MIL-C-26655	6
1		788C016H01	V	CAPACITOR, C2		7
28		1N914		DIODE, CR1 TO CR28	MIL-S-19500/116A	8
4		RC07GF472K		RESISTOR, R1, R5, R10, R14	MIL-R-11	9
8		2N2481		TRANSISTOR, Q1 TO Q8	MIL-S-19500/268A	10
4		CK05CW101K		CAPACITOR, C3, C4, C5, C6	MIL-C-11015	11
12		RC07GF103K		RESISTOR - R2, R3, R4, R6, R7, R8, [redacted], R11, R12, R13, R15, R16, R17	MIL-R-11	12

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

NOTES

(1) ORDER PURCHASED PARTS TO COMPLY WITH T-673303

(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP 12 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

(3) DIP SOLDER PER PS 291944-1

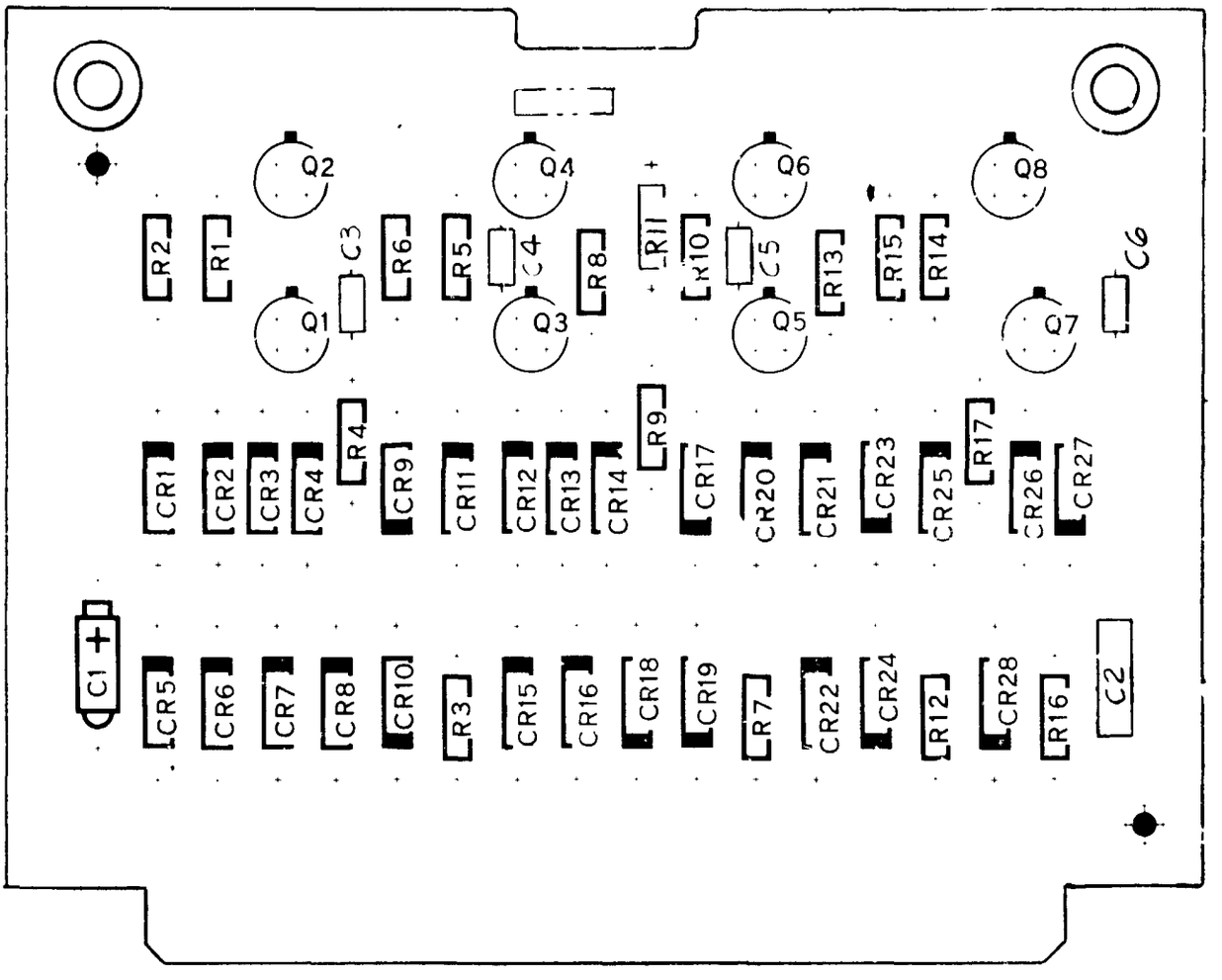
(4) FOR MIL EQUIVALENTS SEE DWG 385A000

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	DWG RELEASED D SPEC 732031		

C-10

CODE IDENT NO	SIZE	DWG NO	
89661	B	PL 3320284 G01	
SCALE —		SHEET 2	

FORM NO BA 5381 2



Westinghouse Electric Corporation		
DEFENSE CENTER (W) BALTIMORE MD., U. S. A.		
TITLE PRINTED WIRING ASSEMBLY NS4-BUFFERS		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3320284

ORIGINAL DATE OF DWG		APPD	
DRAFTSMAN	CHECKED	APPD	
SPECIFICATION		TYPE-MOD-SERIES	
GOVT			
CONTR			
CONTRACT NO			

Westinghouse Electric Corporation

DEFENSE AND SPACE CENTER — BALTIMORE MARYLAND 21203 U S A

DESIGN ACTIVITY APPROVAL

PROCURING ACTIVITY APPROVAL

PARTS LIST

89661 PL 3320332 G01 A

CODE IDENT | SHEET 1 OF 2 SHEETS | REV

ITEM NOMENCLATURE

PRINTED WIRING ASSEMBLY
POWER FAILURE DETECTOR & LI DRIVER
NSS

APPLICATION

ASSY IDENT NO	QTY REQD NEXT ASSY	QTY REQD FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	SERIAL NO. FROM	SERIAL NO. THRU

LTR	REVISION DESCRIPTION	DATE	APPD
A	PARTS LIST RELEASED		

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	A														

QTY REQUIRED 301	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO
1		3320332		PRINTED WIRING ASSEMBLY 1 → 2 → 3		1
1		332D331H01		PRINTED WIRING BOARD		2
X				TEST SPEC		3
X				DIAGRAM SCHEMATIC		4
2		331C264H34	V	EYELET		5
5		RC07GF332K		RESISTOR - R1, R2, R4, R8, R10	MIL-R-11	6
3		RC07GF102K		RESISTOR - R3, R9, R13	MIL-R-11	7
7		RC07GF103K		RESISTOR - R5, R6, R7, R11, R12, R14, R15	MIL-R-11	8
1		RC07GF101K		RESISTOR - R16	MIL-R-11	9
5		C013BC107K		CAPACITOR - C1 TO C5	MIL-C-26655	10
2		788C016H01	V	CAPACITOR - C6, C7		11
1		C013BD275K		CAPACITOR - C8	MIL-C-26655	12
6		1N914		DIODE - CR1 TO CR6	MIL-S-19500/116	13
6		2N2481		TRANSISTOR - Q1 TO Q6	MIL-S-19500/268	14
1		2N1132		TRANSISTOR - Q7	MIL-S-19500/177	15
Y		161P758		PRINTED WIRING MASTER		16

SYMBOLS, V - VENDOR ITEM B - BULK MATERIAL

REVISIONS			
SYM	DESCRIPTION	DATE	APPR'VD
A	DWG RELEASED D 732034		

NOTES

(1) ORDER PURCHASED PARTS TO COMPLY WITH T 673303

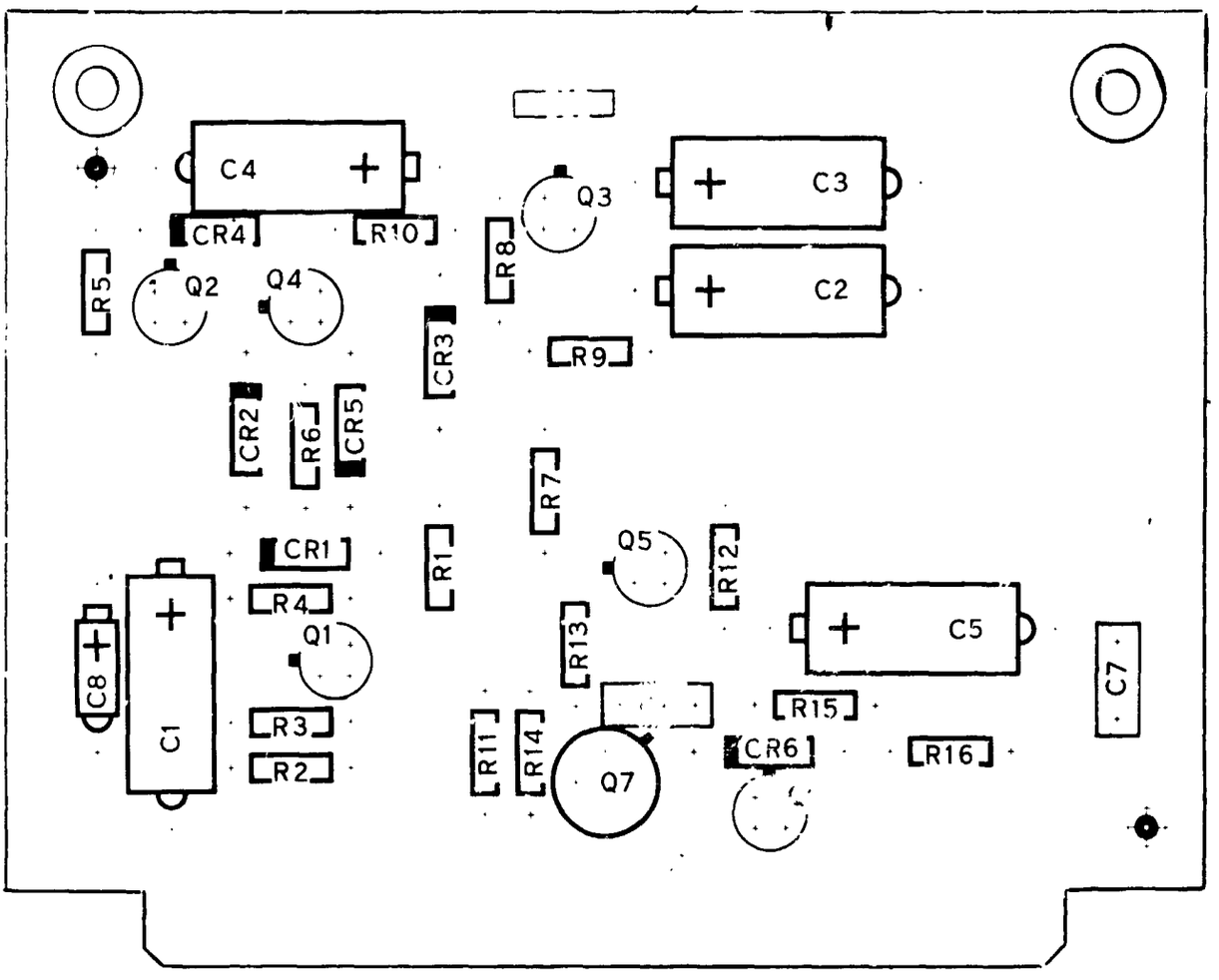
(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP i2 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

3 · DIP SOLDER PER PS 291944 1

(4) FOR MIL EQUIVALENTS SEE DWG 385A000

C-13

89661	B	NO PL 332D332G01	



Westinghouse Electric Corporation		
DEFENSE CENTER (W) BALTIMORE MD., U. S. A.		
TITLE PRINTED WIRING ASSEMBLY POWER FAILURE DETECTOR & SET DRIVER		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3320332

ORIGINAL DATE OF DWG 7 APR 66	APPD	**Westinghouse Electric Corporation**	**PARTS LIST**
DRAFTSMAN J. [illegible]	CHECKED McCrillis	APPD	DEFENSE AND SPACE CENTER (W) BALTIMORE MARYLAND 21203 U.S.A.	**89661 PL 332D294G1** A
	SPECIFICATION	TYPE-MOD-SERIES		CODE IDENT: SHEET 1 OF 2 SHEETS: REV
GOVT			DESIGN ACTIVITY APPROVAL	ITEM NOMENCLATURE: PRINTED WIRING ASSY RELAY DRIVER & RELAY NSG
CONTR			PROCURING ACTIVITY APPROVAL	
CONTRACT NO				

APPLICATION						
ASSY IDENT NO.	QTY. REQD. NEXT ASSY	QTY. REQD. FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	SERIAL NO. FROM	SERIAL NO. THRU

LTR	REVISION DESCRIPTION	DATE	APPD
A	PARTS LIST RELEASED	4-18-66	[illegible]

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8

QTY REQUIRED G01	CODE IDENT	PART NUMBER	MAT'L	DESCRIPTION	SPECIFICATION	ITEM NO
X		332D294		ASSEMBLY (1) THRU 4		1
1		332D293H01		PRINTED WIRING BOARD		2
X				TEST SPEC		3
X				SCHEMATIC		4
2		331C264H34	V	EYELET		5
~~1~~		~~[illegible]~~		~~[illegible]~~		6
~~1~~		~~[illegible]~~		~~[illegible]~~		7
1		CS13BE106K		CAPACITOR C1	MIL-C-26655	8
1		CL65BK500MPC		CAPACITOR C2	MIL-C-3965	9
1		CK05CW101K		CAPACITOR C3	MIL-C-11015	10
1		788C016H01	V	CAPACITOR C4		11
1		CS13BD275K		CAPACITOR C5	MIL-C-26655	12
1		2N1132		TRANSISTOR Q1	MIL-S-19500/177[illegible]	13
1		2N2481		TRANSISTOR Q2	MIL-S-19500/[illegible]FA	14
12		1N914		DIODE CR1 TO CR12	MIL-S-19500/116	15
1		332D342H04	V	RELAY K1		16
3		RC07GF332K		RESISTOR R1,R2,R7	MIL-R-11	17
3		RC07GF102K		RESISTOR R3,R4,R5	MIL-R-11	18
1		RC07GF103K		RESISTOR R6	MIL-R-11	19
1		330C959H17	V	CLIP		20
2		331C264H02	V	EYELET		21

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

NOTES

(1) ORDER PURCHASED PARTS TO COMPLY WITH T-673303

(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP 12 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

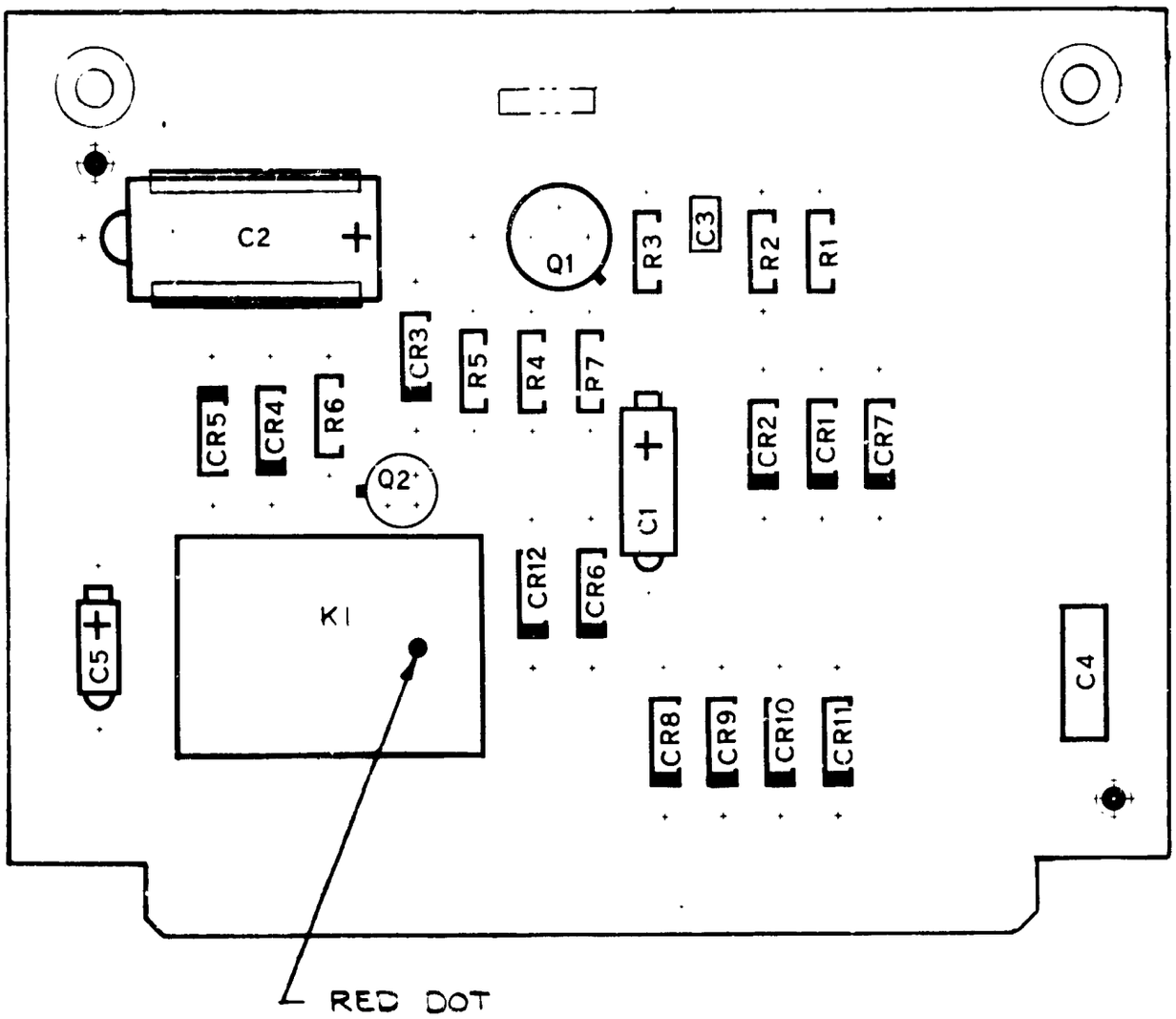
(3) DIP SOLDER PER PS 291944-1

(4) FOR MIL EQUIVALENTS SEE DWG 385A000

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	DRAWING RELEASED DSGN SPEC 732030		

C-16

CODE IDENT NO	SIZE	DWG NO
89661	B	PL332D294G01
SCALE		SHEET 2



Westinghouse Electric Corporation		
DEFENSE CENTER		BALTIMORE MD., U. S. A.
TITLE PRINTED WIRING ASSEMBLY RELAY DRIVER & RELAY		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3320294

ORIGINAL DATE OF DWG	APPD	**Westinghouse Electric Corporation**	**PARTS LIST**
DRAFTSMAN	CHECKED / APPD	DEFENSE AND SPACE CENTER — BALTIMORE MARYLAND 21203 U S A	89661 PL 3320329G01 A
			CODE IDENT — SHEET 1 OF SHEETS — REV
	SPECIFICATION / TYPE-MOD-SERIES	DESIGN ACTIVITY APPROVAL	ITEM NOMENCLATURE
GOVT			PRINTED WIRING ASSEMBLY
CONTR		PROCURING ACTIVITY APPROVAL	DIGITAL DIFFERENCE DETECTOR V-7
CONTRACT NO			

APPLICATION

ASSY IDENT NO	QTY REQD NEXT ASSY	QTY REQD FINAL ASSY	NEXT ASSY	USED ON CONTRACT END ITEM	SERIAL NO FROM	SERIAL NO THRU

LTR	REVISION DESCRIPTION	DATE	APPD
A	PARTS LIST RELEASED		

REVISION STATUS OF EACH SHEET

1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
A	A														

QTY REQUIRED .01	CODE IDENT	PART NUMBER	SYM	DESCRIPTION	SPECIFICATION	ITEM NO
1		3320329		PRINTED WIRING ASSEMBLY 1 → 2 → 3		1
1		3320329H01		PRINTED WIRING BOARD		2
				TEST SPEC		3
				DIAGRAM SCHEMATIC		4
		10264H34	V	EYELET		5
2		(5)		CAPACITOR - C1, C2		6
18		1N914		DIODE - CR1 - CR18	MIL-S-19500/116	7
2		2N2421		TRANSISTOR - Q1, Q2	MIL-S-19500/ 68	8
10		C0715F[illegible]2K		RESISTOR - R1, R4, R5, R6, R7, R8, R11 [illegible], R13, R14	MIL-R-11	9
4		C0715F10[illegible]K		RESISTOR - R2, R3, R9, R10 [illegible]	MIL-R-11	10
4		1280075H01	V	MICROELECTRONIC DEVICE Z1, Z2, Z3, Z4		11
1		C 1380[illegible]27[illegible]		CAPACITOR - C3	MIL-C-2665[illegible]	12
1		7 [illegible]6C016H01	V	CAPACITOR - C4		13
X		[illegible]		[illegible] - MAGNET		14

SYMBOLS: V - VENDOR ITEM B - BULK MATERIAL

FORM NO. RA 5188

WR4L/AT

PK

NOTES

(1) ORDER PURCHASED PARTS TO COMPLY WITH T-673303

(2) MANUFACTURING SECTION APPLY SERIAL NUMBER OBTAINED FROM PRODUCTION PLANNING FOR EACH UNIT MANUFACTURED RUBBER STAMP 12 HIGH CHARACTERS APPROX AS SHOWN PER FS 184K (BLACK)

(3) DIP SOLDER PER PS 291944-1

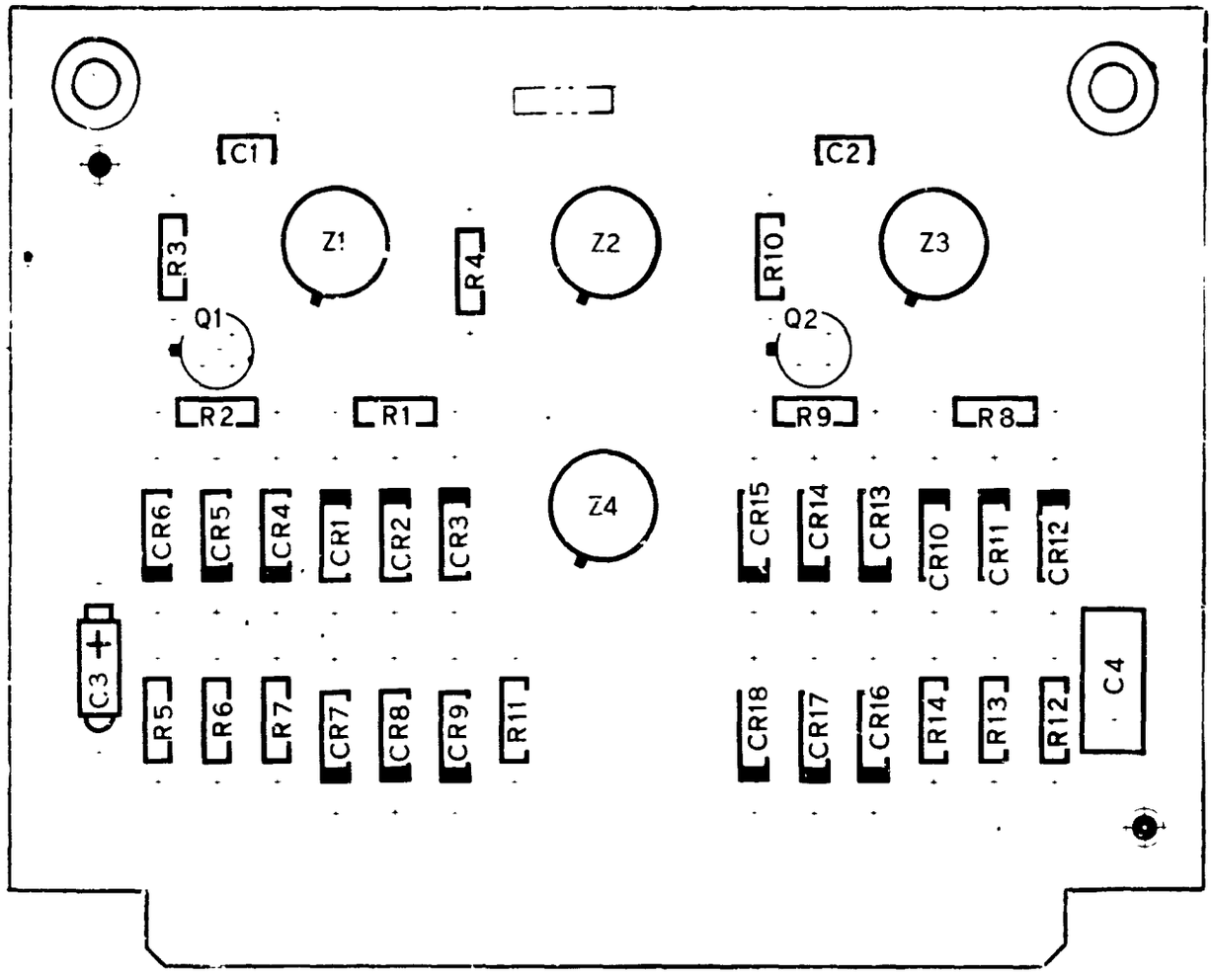
(4) FOR MIL EQUIVALENTS SEE DWG 385A000

(5) *ELECTRON PRODUCTS, THEIR PT. NO. EPC04X182-M*

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	*DWG RELEASED DSGN SPE 732033*		

C-19

CODE IDENT NO	SIZE	DWG NO
89661	B	332D329G01
SCALE		SHEET 2



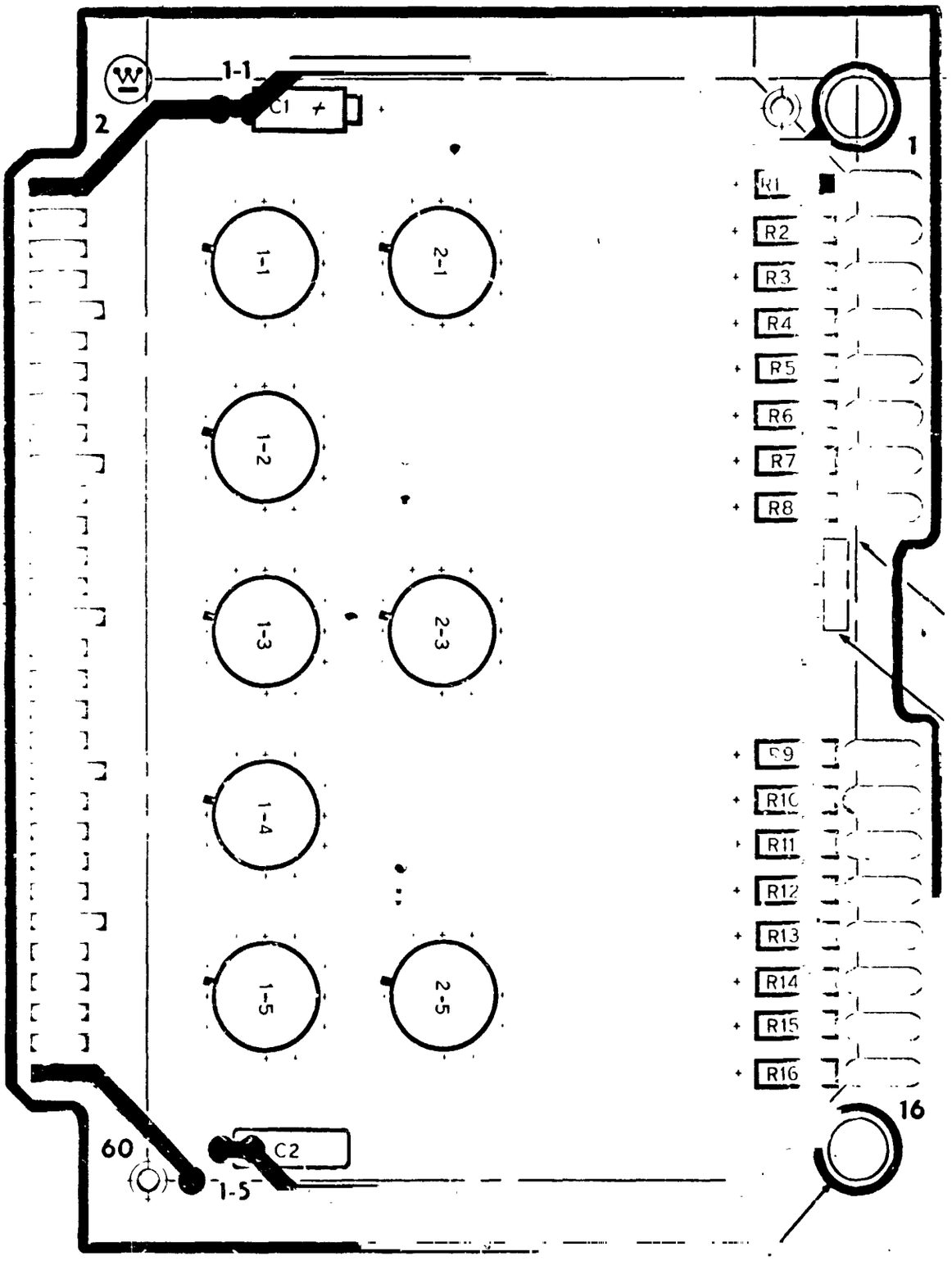
Westinghouse Electric Corporation		
DEFENSE CENTER (W) BALTIMORE MD., U. S. A.		
TITLE PRINTED WIRING ASSEMBLY DIGITAL DIFFERENCE DETECTOR		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3320329

FIGURE C-2. PRINTED WIRING ASSEMBLY PARTS LIST

NAND Gate Logic -002, 002A

(Drawing # 33CD002)

QUANTITY REQUIRED	PART NO.	DESCRIPTION	SPECIFICATION
X	330D002	Assembly	
1	330D001H01	Printed wiring board	
2	331C264H34	Eyelet	
16	RC07GF103K	Resistor R1 - R16 (Type 002 only)	MIL-R-11
1	CS13BD275K	Capacitor C1 (Type 002 only)	MIL-C-26655
1	788C016H01	Capacitor C2 (Type 002 only)	
8	128C362H01	Microelectronic Device RM6177;1-1, 1-2,1-3,1-4,1-5, 2-1, 2-3, 2-5	



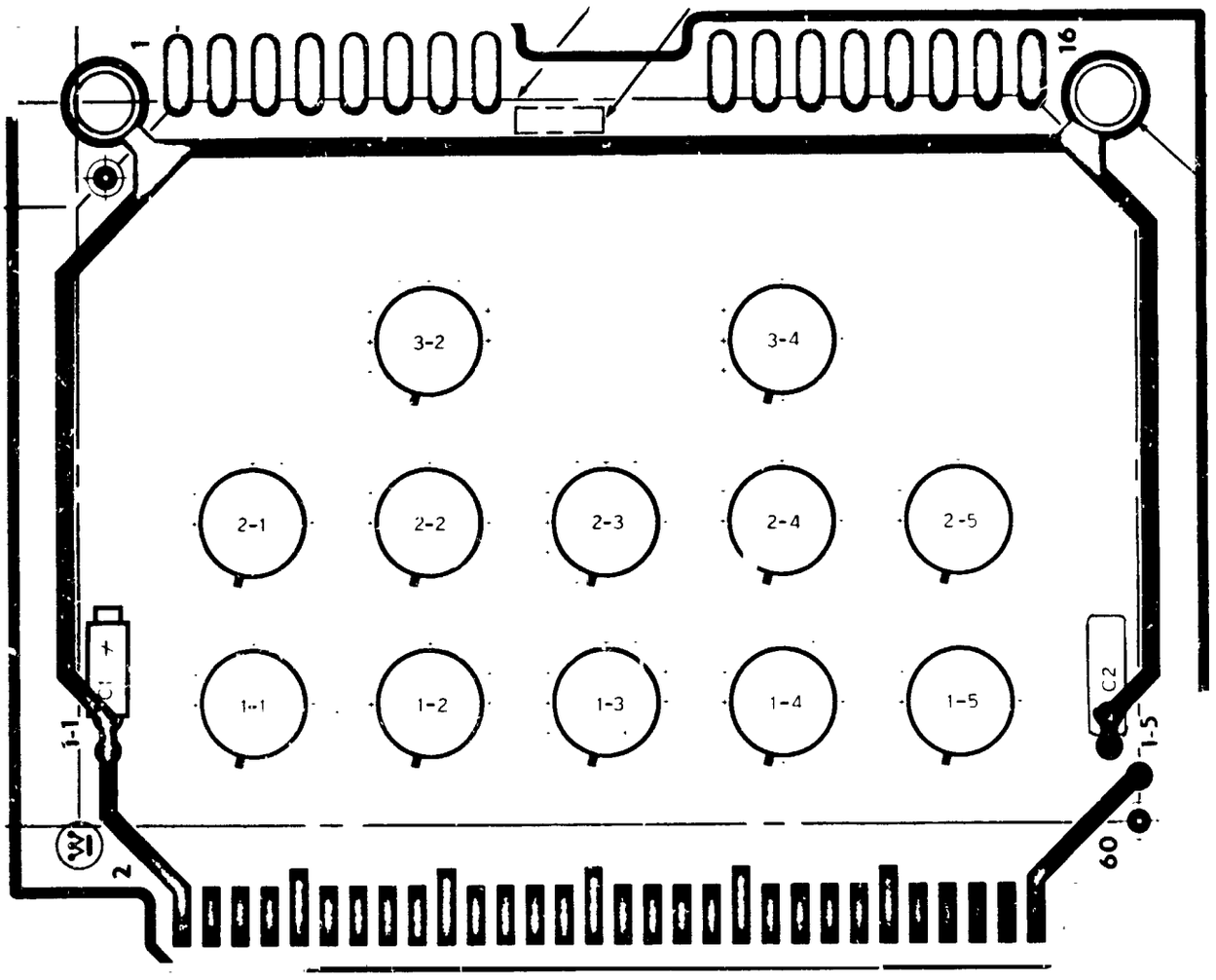
Westinghouse Electric Corporation		
DEFENSE CENTER		BALTIMORE MD., U.S.A.
TITLE: PRINTED WIRING ASSEMBLY GATE, NAND		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3300002

FIGURE C-3. PRINTED WIRING ASSEMBLY PARTS LIST

PARALLEL REGISTER-004

(DRAWING #330D004)

QUANTITY REQUIRED	PART NUMBER	DESCRIPTION	SPECIFICATION
X	330D004	Assembly	
1	330D003H01	Printed Wiring Board	
2	331C264H34	Eyelet	
1	CS13BD275K	Capacitor C1	MIL-C-26655
1	788C016H01	Capacitor C2	
12	128C073H01	Microelectronic Device RS294T, 1-1, 1-2, 1-3, 1-4, 1-5, 2-1, 2-2, 2-3, 2-4, 2-5, 3-2, 3-4	



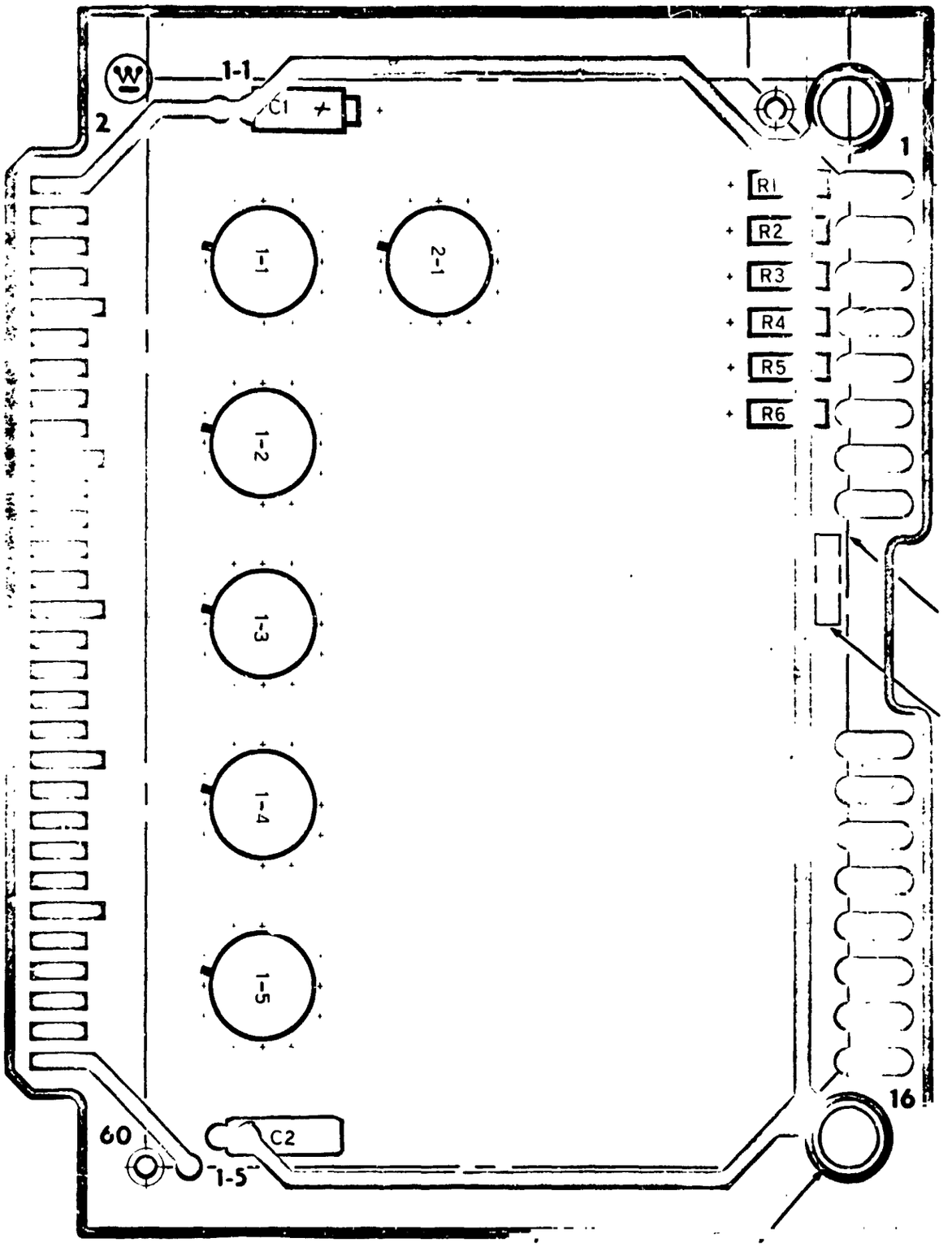
Westinghouse Electric Corporation		
DEFENSE CENTER		BALTIMORE MD., U. S. A.
TITLE: PRINTED WIRING ASSEMBLY REGISTER, PARALLEL		
CODE IDENT NO. 89661	SIZE D	DWG NO. 330D004

FIGURE C-4. PRINTED WIRING ASSEMBLY PARTS LIST

FAN-IN GATE LOGIC-014

(DRAWING #330D014)

QUANTITY REQUIRED	PART NUMBER	DESCRIPTION	SPECIFICATION
X	330D014	Assembly	
1	330D013H01	Printed Wiring Board	
2	331C264H34	Eyelet	
6	RC07GF103K	Resistor R1-R6	MIL-R-11
1	CS13BD275K	Capacitor C1	MIL-C-26655
1	128C362H01	Microelectronic Device RM6177, 1-4	
1	128C075H01	Microelectronic Device RS296T, 1-1	
1	128C077H01	Microelectronic Device RS298T, 1-2	
3	128C078H01	Microelectronic Device RS299T, 1-3, 1-5, 2-1	



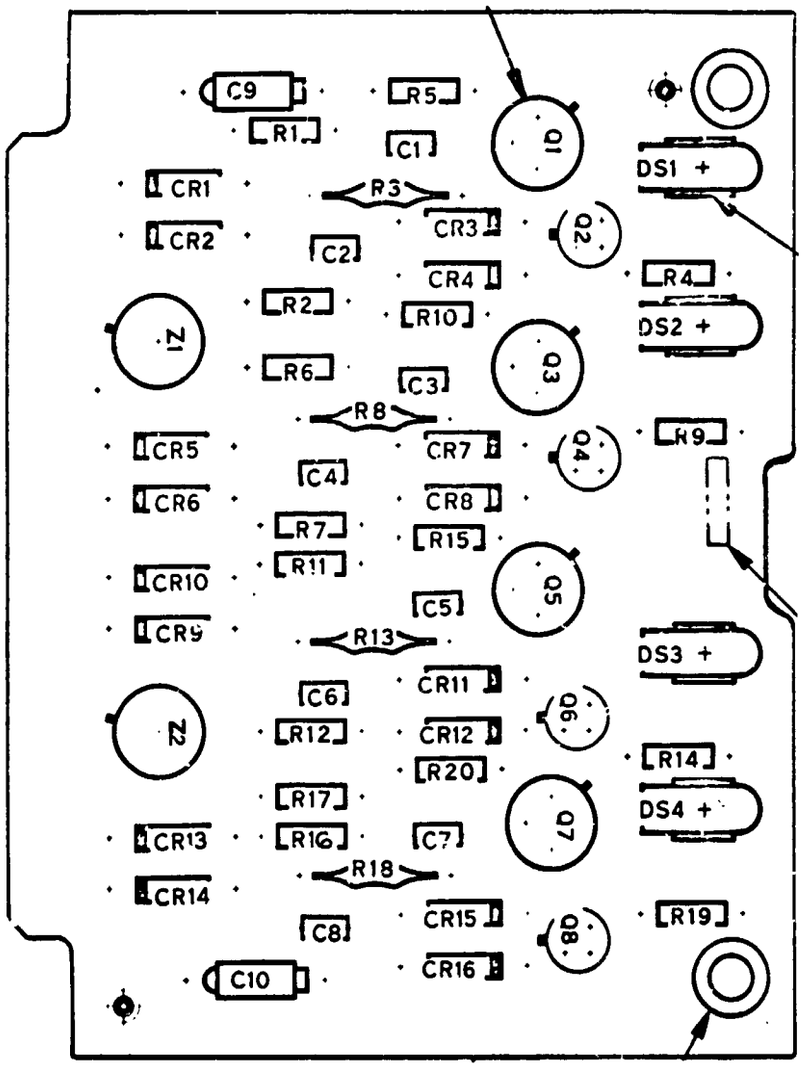
Westinghouse Electric Corporation		
DEFENSE CENTER		BALTIMORE MD., U.S.A.
TITLE: PRINTED WIRING ASSEMBLY GATE, FAN IN		
CODE IDENT NO. 89661	SIZE D	DWG NO. 3300014

FIGURE C-5. PRINTED WIRING ASSEMBLY PARTS LIST

POSITIVE LOGIC DRIVER - 469

(DRAWING #330D469)

QUANTITY REQUIRED	PART NUMBER	DESCRIPTION	SPECIFICATION
X	330D469	Assembly	
1	330D468H01	Printed Wiring Board	
2	331C264H34	Eyelet	
4	RC07GF472K	Resistor R5, R10, R15, R20	MIL-R-11
8	RC07GF152K	Resistor R1, R2, R6, R7, R11, R12, R16, R17	MIL-R-11
4	RC07GF122K	Resistor R3, R8, R13, R18	MIL-R-22684
4	RC07GF332K	Resistor R4, R9, R14, R19	MIL-R-11
8	CK05CW470K	Capacitor C1-C8	
2	CS13BE225M	Capacitor C9, C10	MIL-C-26655
16	1N914	Diode CR1-CR16	MIL-S-19500/116A
4	2N1132	Transistor Q1,Q3, Q5,Q7	MIL-S-19500/177
4	2N2481	Transistor Q2,Q4, Q6,Q8	MIL-S-19500/268
2	128C362H01	Microelectronic Device, RM6177, Dual-3 NAND, Z1, Z2	
4	128C271H01	Ballast Lamp DS1-DS4, Chicago Miniature CM8-634	
4	330C958H40	Clamp	
4	331C264H10	Eyelet	



Westinghouse Electric Corporation		
DEFENSE CENTER		BALTIMORE MD., U. S. A.
TITLE: PRINTED WIRING ASSEMBLY POSITIVE LOGIC DRIVER		
CODE IDENT NO.	SIZE	DWG NO.
89661	D	330D469

FIGURE C-6. PRINTED WIRING ASSEMBLY PARTS LIST

RESISTOR CARD - 030

(DRAWING #330D030)

QUANTITY REQUIRED	PART NUMBER	DESCRIPTION	SPECIFICATION
1	330D029H01	Printed Wiring Board	
2	331C264H34	Eyelet	
11	RC07GF103K	Resistor R1-R11	MIL-R-11
2	788C01GH01	Capacitor C2, C4	
1	CKC5CW102K	Capacitor C3	MIL-C-11015
1	CS13BD275K	Capacitor C1	MIL-C-26655
3	1N914	Diode CR1-CR3	MIL-S-19500/116A

FIGURE C-7. PARTS LIST, REGULATOR

QUANTITY REQUIRED*	PART NUMBER	DESCRIPTION
4	RC42GF620J	Resistor R1-R4
2	CS13BC107K	Capacitor, C1, C2
2	1N3017B	Diode CR1, CR2
2	1N540	Diode CR3, CR4
2	2N1016A	Transistor Q1, Q2

* For one of the three Regulator Circuits used

FIGURE C-8. PARTS LIST, SEQUENCER CHASSIS

Quantity Required	Description
1	Card-Rack Assembly w/Dust Cover
99	Card Connector, Hughes #EMS030DJ000
9	Printed Circuit Card, NS2
6	NS3
12	NS4
3	NS5
9	NS6
7	NS7
7	002
12	002A
4	004
3	014
3	469
3	030
3	+6V Regulator
3	Oscillator
1	Chassis Connector, Amphenol #25-4401-16P
2	Amphenol #57-40500
1	Amphenol #57-40240

FIGURE C-8. PARTS LIST (Concluded)

Quantity Required	Description
9	Fuse 1/4 amp
3	3/4 amp
2	Terminal Block
12	Diode 1N547
2	1N914
3	1N1200
1	1N3997A
9	Resistor, RC20GF751J
1	15 ohm, 10 Watt, wire wound
9	Capacitor, CS13AF100K

FIGURE C-9. PARTS LIST, TEST CHASSIS

Quantity Required	Description
1	Turret Chassis, Bud #60-2366
1	Chassis Panel, Bud # PA-1106
1	Chassis Panel, Bud # PA-1112
1	Chassis Panel, Bud # PS1259
1	Mylar Panel Cover
1	+28V Unregulated Power Supply, Acopian Model US-28
1	+12V Regulated Power Supply, Lamda Model LMC12
1	+8V Unregulated Power Supply
1	Transformer
4	Diode, 1N914
1	Resistor, RC07GF331K
1	Capacitor, CS13AF100K
1	Fuse Holder, Bussman 4405
1	Fuse, 2 amp
26	Indicator Light and Socket, Transistorized
7	TEC #LVN-D12-AL-F2
7	TEC #LVN-D12-A1-F3
12	TEC #LVN-D12-AL-F8

FIGURE C-9. PARTS LIST (Continued)

Quantity Required	Description
9	Indicator Light and Socket, Incandescent, Dailco 10-3830-931
1	Indicator Light and Socket, Neon, Dailco 133-8836-931
3	Switch, Push Button "One-Shot," Micro #1PB625
15	Switch, Push Button, Grayhill #4001
11	Switch, Toggle, SPST Arrow, Hart and Hegeman #6200
8	SPDT Arrow, Hart and Hegeman #6202
6	SPDT-Center Off, Kulka #ST42E
1	SPDT Arrow, Hart and Hegeman #6206
20	Test Point, Tip, Per Westinghouse DWG 328C182-H0-
6	Miniature Coax, per Westinghouse DWG 54B7128-H02
1	Chassis Connector, Amphenol #26-4401-16P
2	Amphenol #57-40500
1	Amphenol #57-40240
2	Cable Connector Amphenol #26-4301-16S
2	Amphenol #57-30500
2	Amphenol #57-30240

FIGURE C-9. PARTS LIST (Concluded)

Quantity Required	Description
2	Socket, Octal, Amphenol
1	Plug, Octal, Amphenol
2	Cable Cap, Clamp, Amphenol
1	Line Cord, a.c.
1	Plug, a.c., 2-prong
25	Resistor, RC07GF121J
2	RC07GF150J
12	RC07GF100J
6	RC07GF101K
3	Capacitor, 788C016H01 (0.01 uf)
25	Ceramic Disc. (1 uf.)

Note: Sequencer and Test Chassis interconnected by one 16 wire (# 18 gauge) power cable, one 24 wire (#24 gauge) signal cable, two 50 wire (#24 gauge) signal cables